

COMPAL CONFIDENTIAL

MODEL NAME : LOKI N3V3 KBL UMA

PCB NO : DA60022P010

BOM P/N : 431AET31L01~L10&L51~L57

KBL-U & R + MEC1416 board 2018-11-06

REV : 1.0 (A00)

PCB R1

ZZZ
DA60022P010
PCBR1@
PCB 2EI LA-G714P REV1 M/B 5

DAZ R1

ZZZ
DAZ2EI00200
DAZR1@
PCB EDI72 LA-G714P LS-F112P/F114P/F117P

DAZ R3

ZZZ
DAZ2EI00201
DAZR3@
PCB EDI72 LA-G714P LS-F112P GOLD A31

X4E#

ZZZ
X4EAET31L51
100@X4E@
SMT EMC N3 KBL UMA EE AG714 EDI73

X4E#

ZZZ
X4EAET31L01
1000@X4E@
SMT EMC N3V3 KBL UMA EE AG714 EDI72

KBL R3

UC1
SA0000A377L
i5KBLU_R3@
S IC FJ8067702739739 SR342 H0 2.5G A311

UC1
SA0000BLD1L
i3KBLU42_SMB0_R3@
S IC FJ8067703282620 SR3LD Y0 2.3G A311

UC1
SA0000BYB1L
i3KBLU23_SMB0_R3@
S IC FH8067703037315 SR3N6 J1 2.3G A311

UC1
SA0000A346L
i7KBLU_R3@
S IC FJ8067702739740 SR341 H0 2.7G A311

UC1
SA0000ADL3L
KBLU_Celeron_R3@
S IC FJ8067702739933 SR349 H0 1.8G A311

UC1
SA0000ADV3L
KBLU_Pentium_R3@
S IC FJ8067702739932 SR348 H0 2.3G A311

UC1
SA0000BKN3L
i3KBLR_R3@
S IC FJ8067703282227 SR3W0 Y0 2.2G A311

UC1
SA0000AWB3L
i5KBLR_R3@
S IC FJ8067703282221 SR3LB Y0 1.6G A311

UC1
SA0000AWC2L
i7KBLR_R3@
S IC FJ8067703281816 SR3LC Y0 1.8G A311

UC1
SA0000BLH1L
i3KBLU22_SMB0_R3@
S IC FJ8067702739769 SR3TK H0 2.3G A311

@ : Un-pop Component
UMA@/DIS@ : UMA & DIS Type
U22@/U42@ : KBL U/KBL U-R
EC@ : EC
JP@/PJP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
TPM@/FTPM@ : HW TPM/SW TPM
MMC@ : eMMC
FFS@ : Free Fall Sensor
MODS@ : Modern Standby

Layout Dell logo



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REV: X00
PWB: 9HTP8

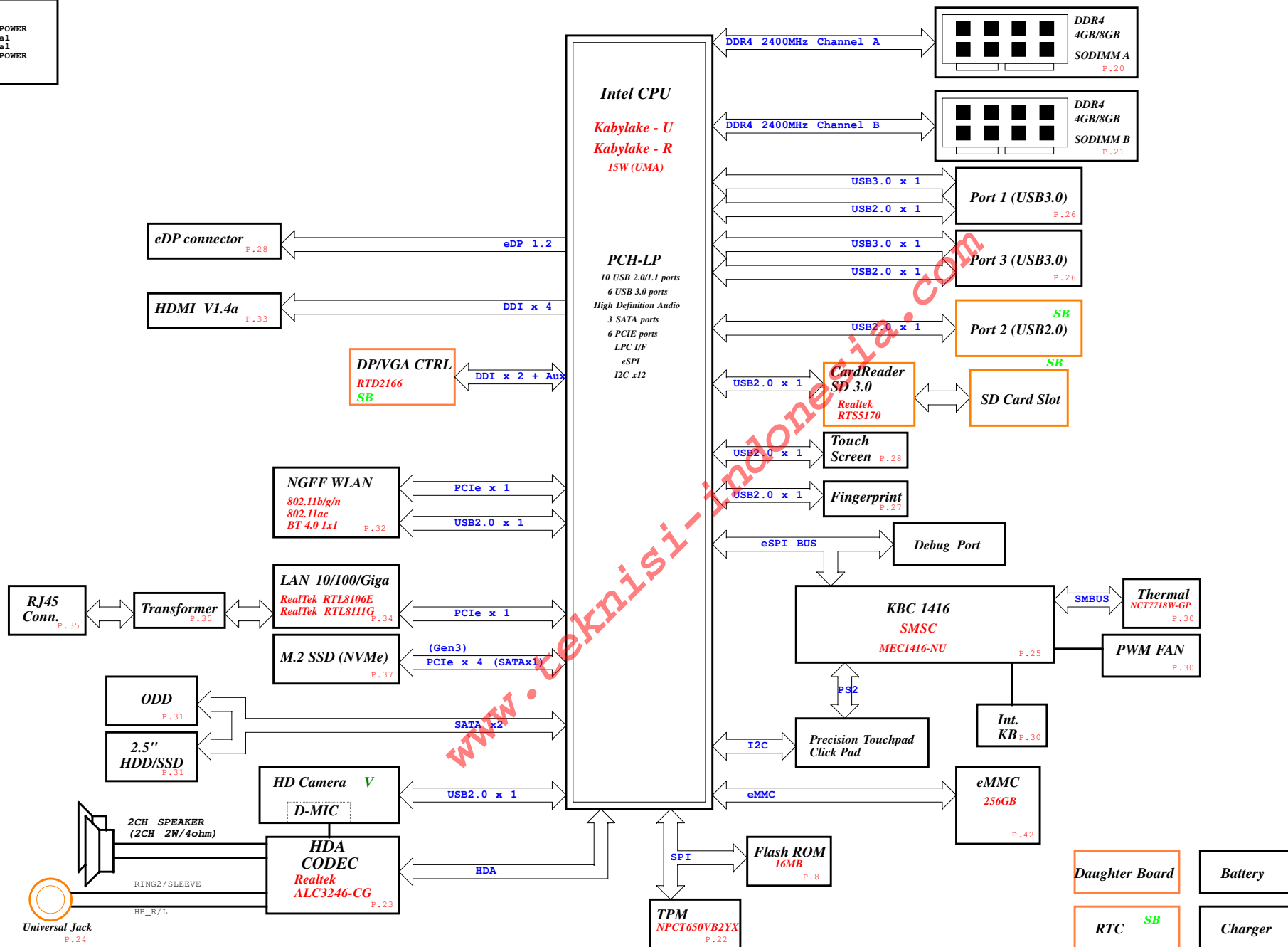
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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title	
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PCB Stack

1.0mm/6L

L1: TOP
L2: GND/POWER
L3: Signal
L4: Signal
L5: GND/POWER
L6: BOT

Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
1	USB2.0 Port1
2	USB2.0 Port2 , IO/B
3	USB2.0 Port3
4	NC
5	CCD
6	Card Reader IO/B
7	BT
8	Touch Screen
9	Finger Printer
10	NC

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1			USB3.0 Port1
USB3.0-2			NC
USB3.0-3			USB3.0 Port3
USB3.0-4			NC
USB3.0-5	PCIE-1		NC
USB3.0-6	PCIE-2		NC
	PCIE-3		NC
	PCIE-4		NC
	PCIE-5		10/100M LAN
	PCIE-6		WLAN
	PCIE-7	SATA-0	SATA HDD
	PCIE-8	SATA-1	SATA ODD
	PCIE-9		NVME SSD
	PCIE-10		NVME SSD
	PCIE-11	SATA-1*	NVME SSD
	PCIE-12	SATA-2	NVME SSD

PM TABLE

<div>power plane</div> <div>State</div>	+RTC_CELL	B+	+1.0V_PRIM +1.0V_MPHYGT +1.8V_PRIM +3VALW +3VALW_PCH +3.3V_ALW_DSW +5VALW	+1.0V_VCCST +1.2V_DDR +2.5V_MEM	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VGA_CORE +VCC_CORE +0.6V_DDR_VTT
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
M3	ON	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	ON	OFF	OFF
S4&S5 / AC doesn't exist	ON	ON	OFF	OFF	OFF
G3	ON	OFF	OFF	OFF	OFF

Board ID table

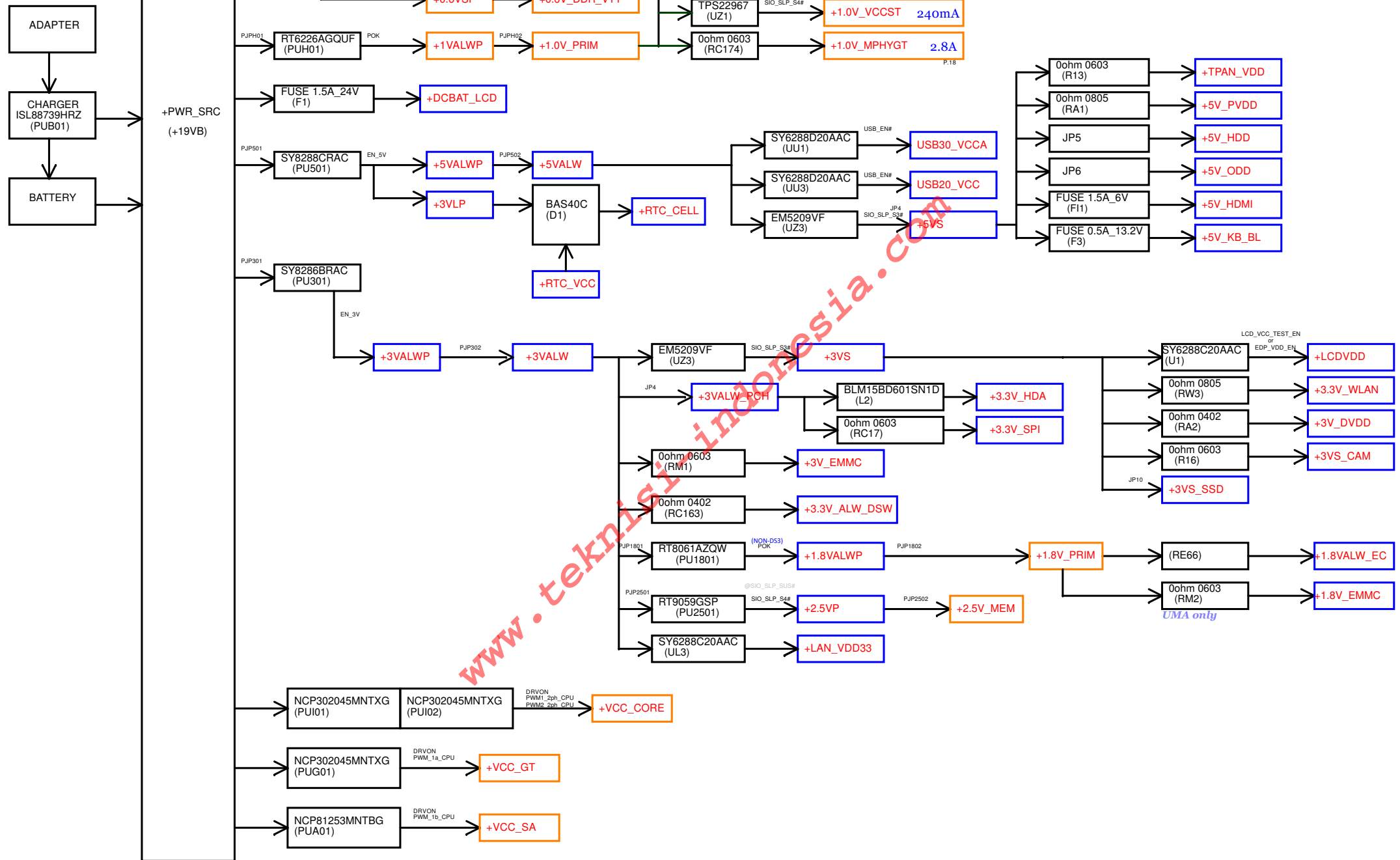
Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10K	3.000	EVT
2	100	17.8K	2.801	DVT1
3	100	27K	2.598	DVT2
4	100	37.4K	2.402	
5	100	49.9K	2.201	Pilot
6	100	64.9K	2.001	
7	100	82.5K	1.808	
8	100	107K	1.594	
9	100	154K	1.299	
10	100	200K	1.1	
11	100	TBD	0.9	
12	100	TBD	0.7	
13	100	TBD	0.5	
14	100	TBD	0.3	

High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP

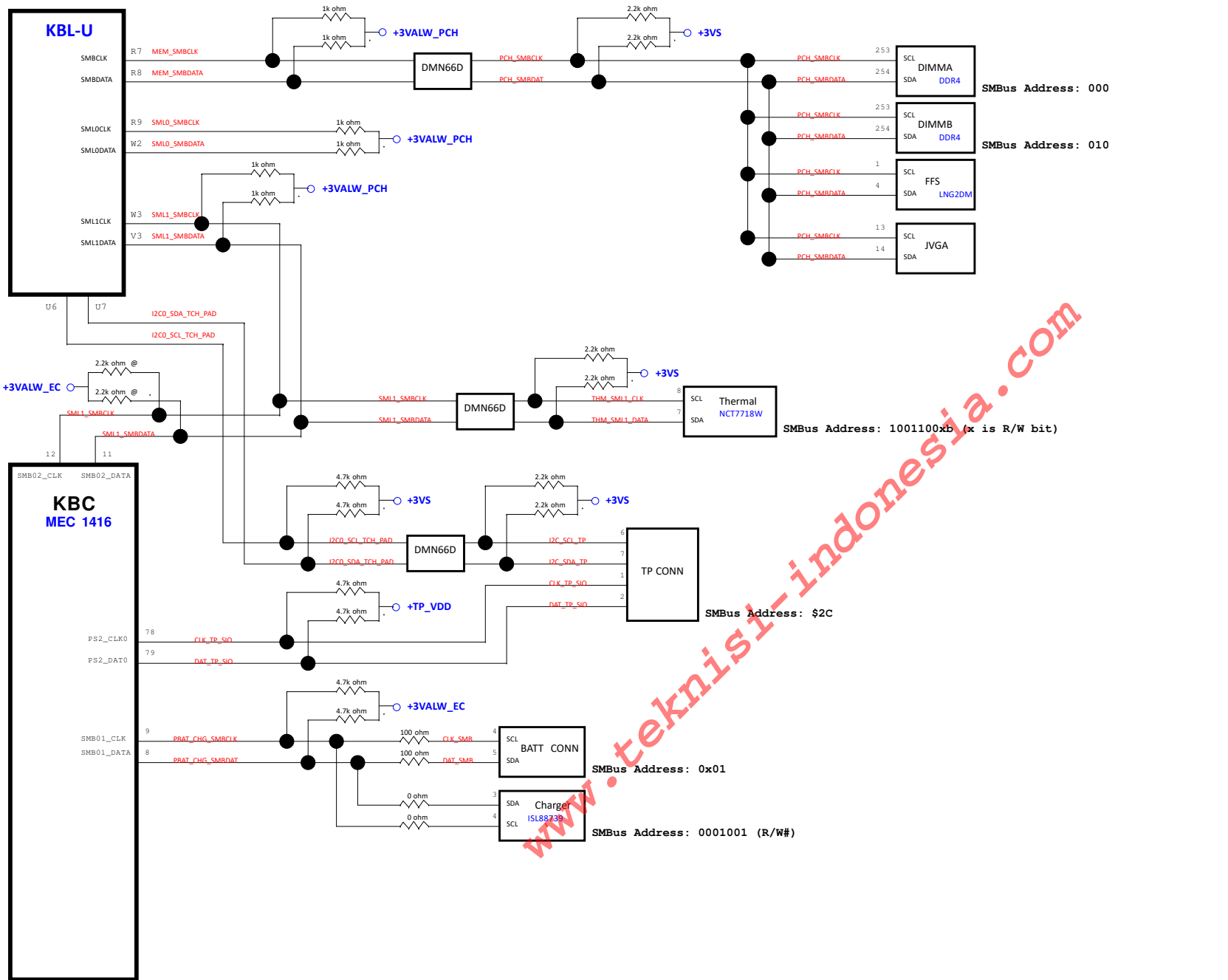
2	3	4	5	6	7	8	9	10	11	12	13	14	15	16				
USB3 #1 (Capable of OTG)	USB3 #2	USB3 #3	USB3 #4	USB3 #5	USB3 #6	PCIe #3	PCIe #4	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12			
				PCIe #1	PCIe #2	GPE	GPE	GPE	SATA #1A	SATA #1B	GPE	GPE	SATA #2					
														X4	X2	X2	X4	X2
				X4				X4				X4		X2				
								Intel® RST for PCIe Storage				Intel® RST for PCIe Storage						

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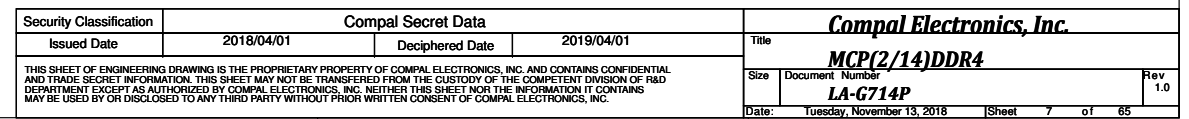
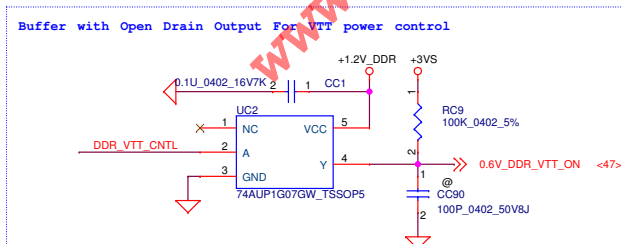
CPU PWR
Peripheral Device PWR



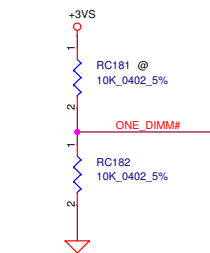
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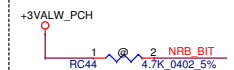
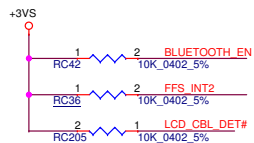
DDR4 Interleaved Memory



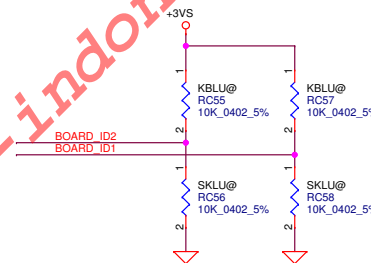
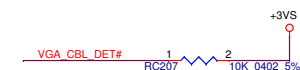
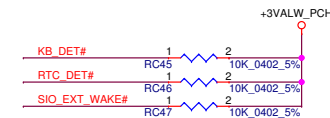
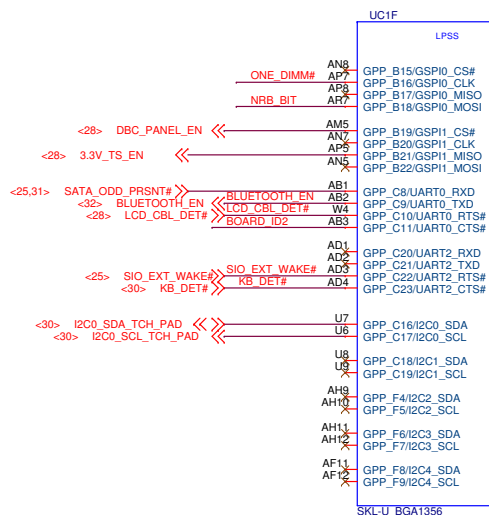
Main Func = CPU



DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM



NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE
Weak IPD	



CPU ID (PCBA VRAM Size Config.)	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
KBL-U	1	1
KBL-R	1	0
Reserved	0	1
SKL-U	0	0

RC55 KBLR@
10K_0402_5%
SD028100280

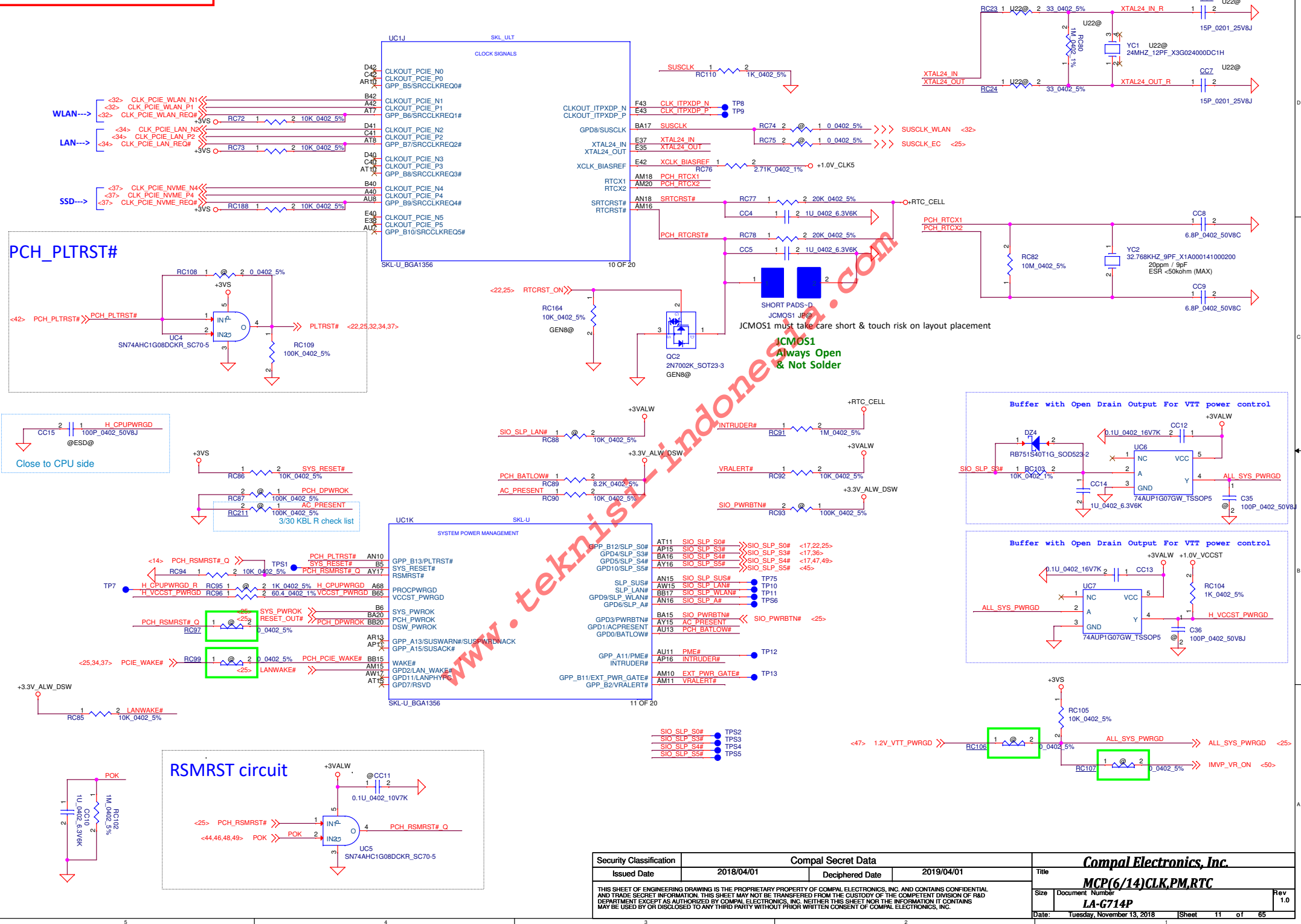
RC58 KBLR@
10K_0402_5%
SD028100280

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				Deciphered Date				MCP(4/14)GSPI,I2C,UART,ISH			
				2019/04/01				Size			
								Document Number			
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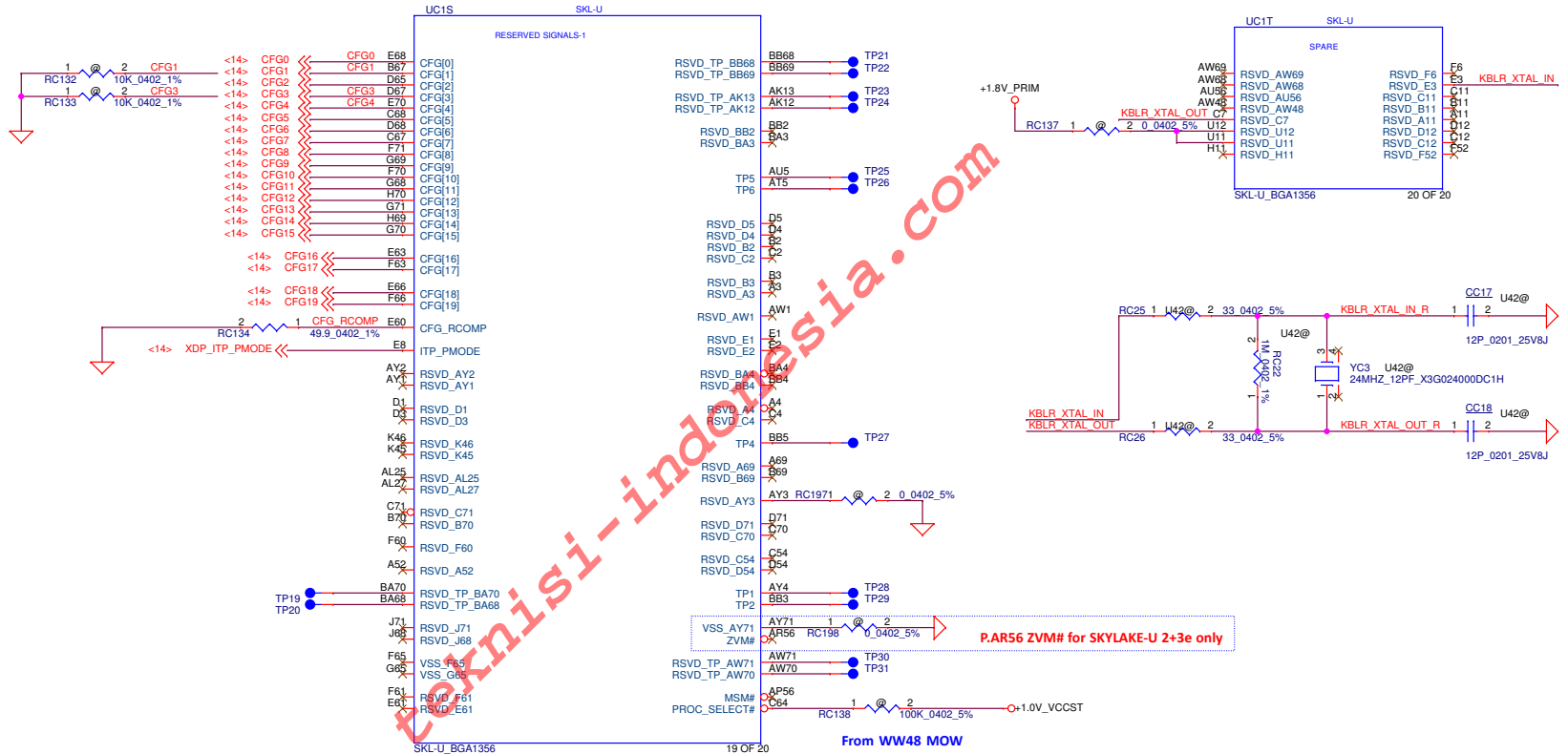
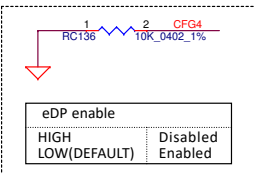
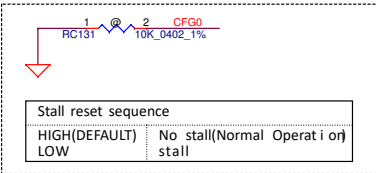
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Main Func = CPU

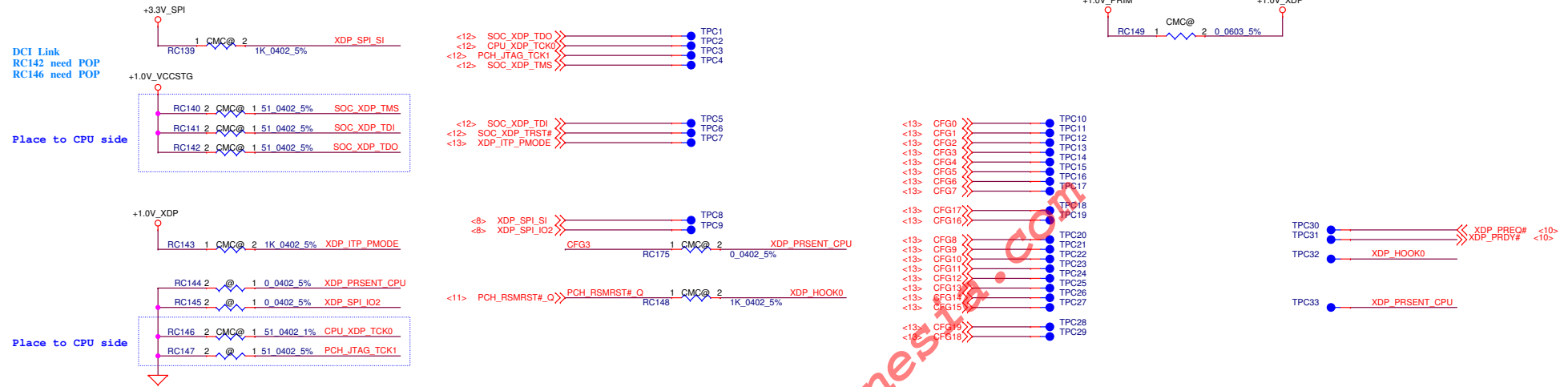


Main Func = CPU



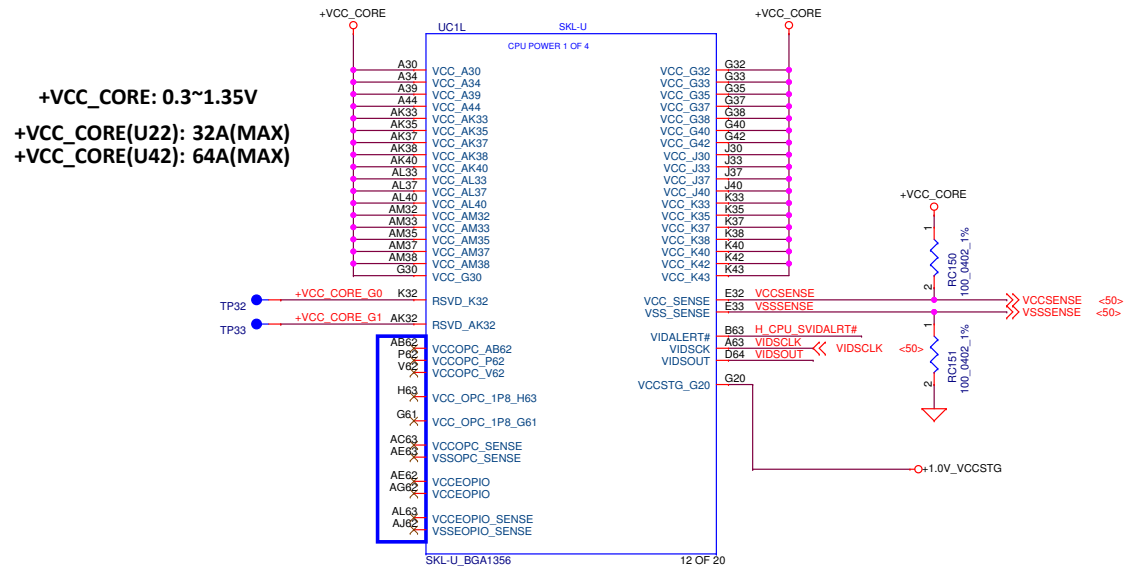
Connector Less Routing Topology

PRIMARY CMC CONN



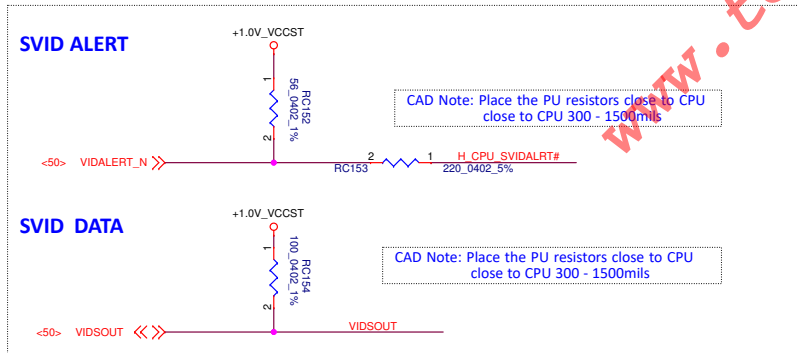
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Main Func = CPU



PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

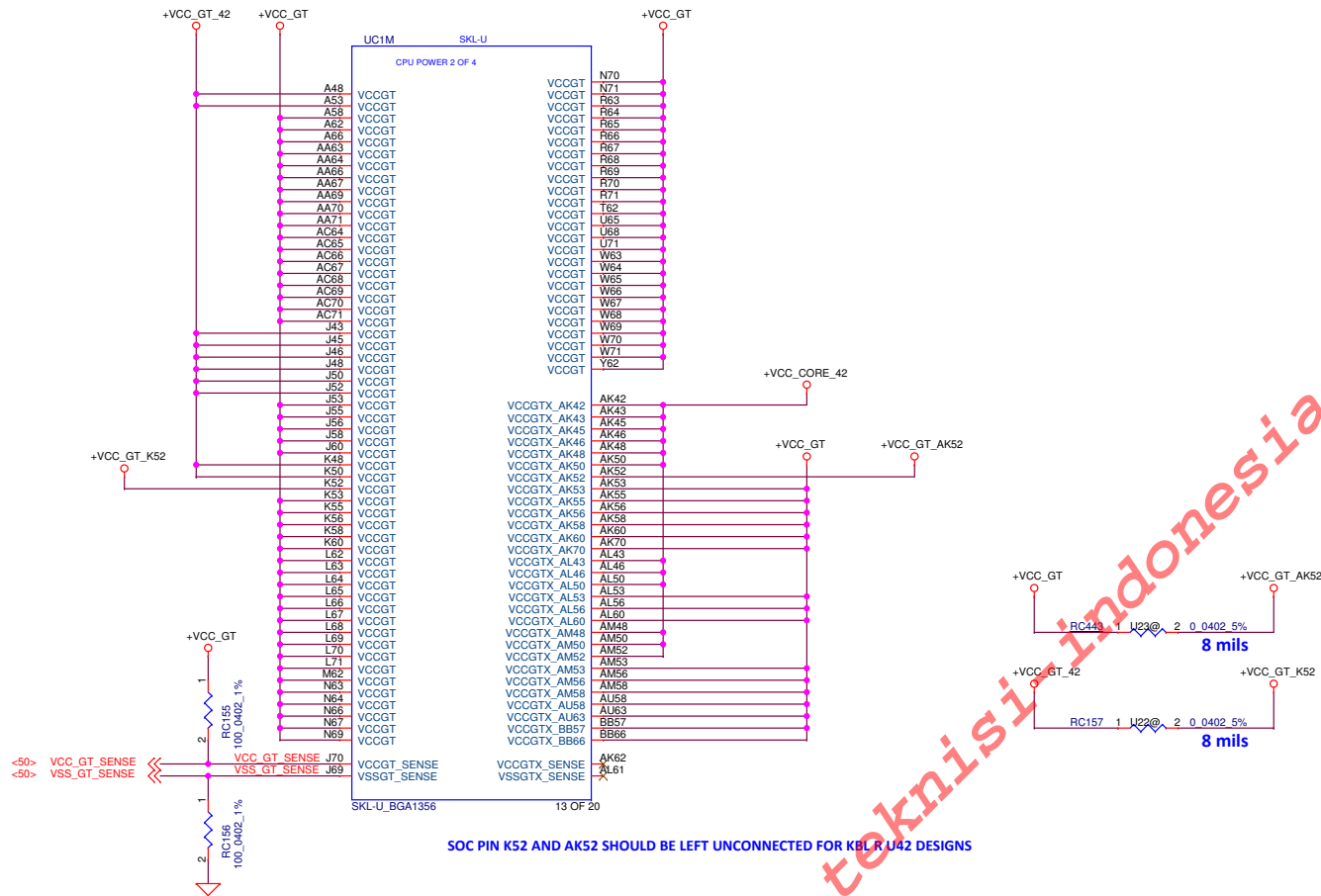


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				Size	Document Number
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Main Func = CPU

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V

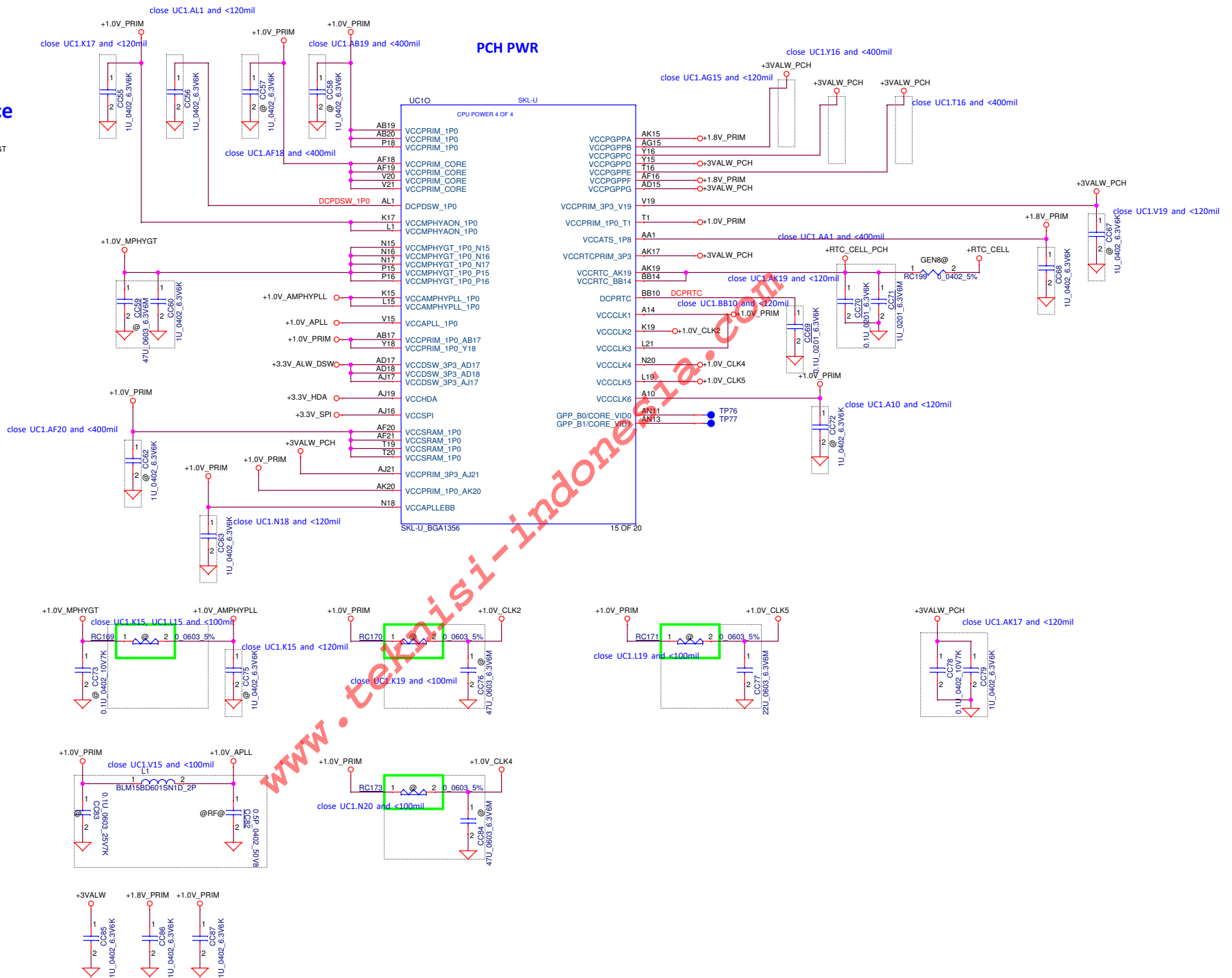
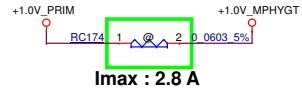
+VCC_GT(U22): 31A(MAX)
+VCC_GT(U42): 28A(MAX)



SOC PIN K52 AND AK52 SHOULD BE LEFT UNCONNECTED FOR KBL R U42 DESIGNS

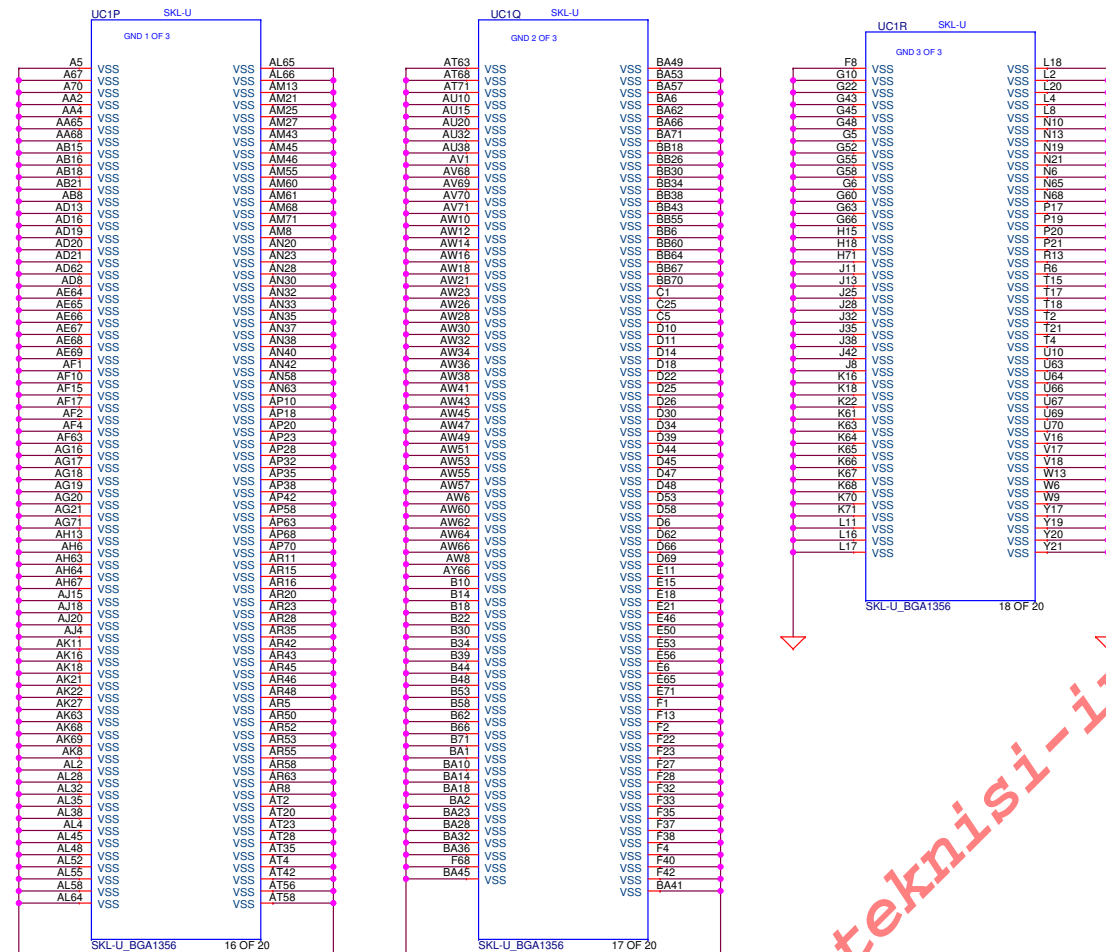
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+1.0V_MPHYGT source



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Main Func = CPU



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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				LA-G714P	
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Main Func = DDR

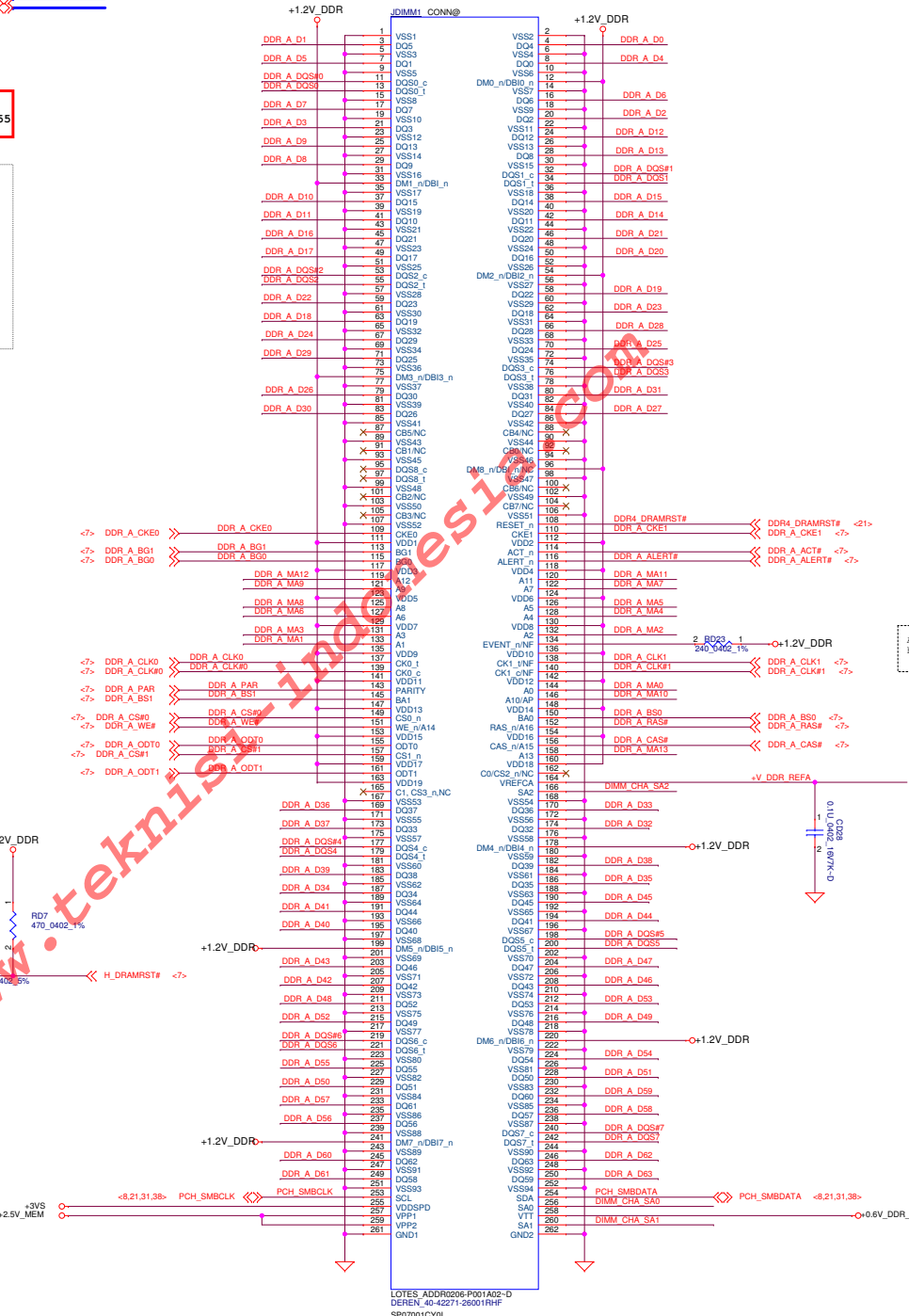
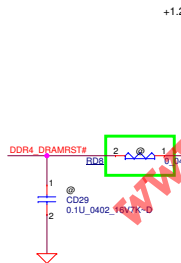
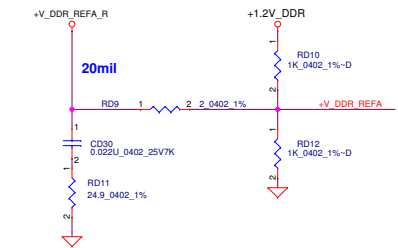
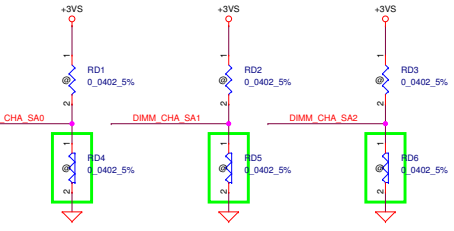
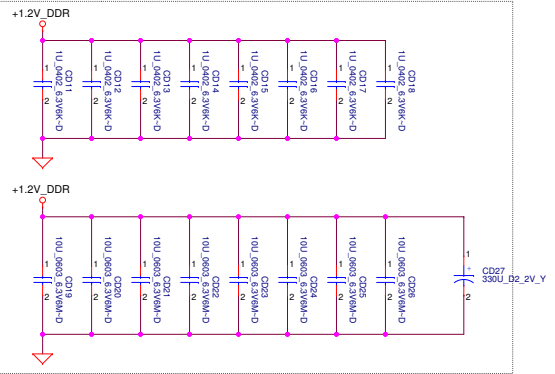
<7> DDR_A_D0_63J
<7> DDR_A_MA(0..13)
<7> DDR_A_DQS#0..7
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Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

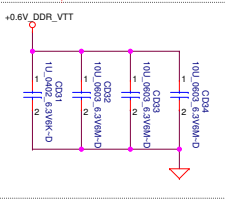
Layout Note:
Place near JDIMM1



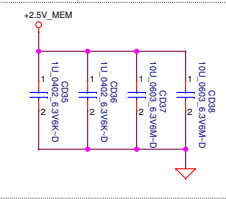
All VREF traces should
have 10 mil trace width

Main Func = DDR

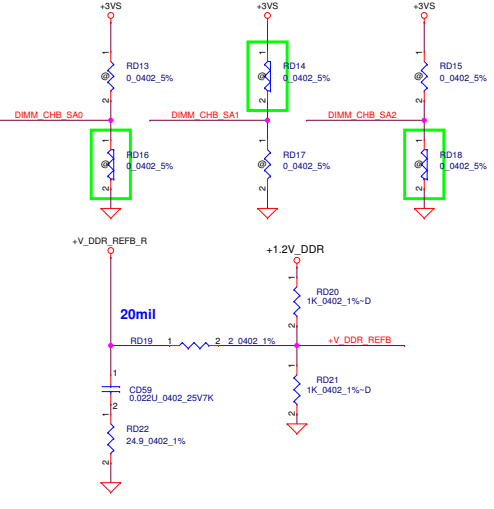
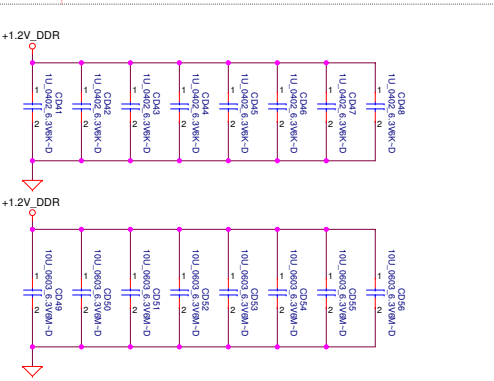
Layout Note:
Place near JDIMM2.258



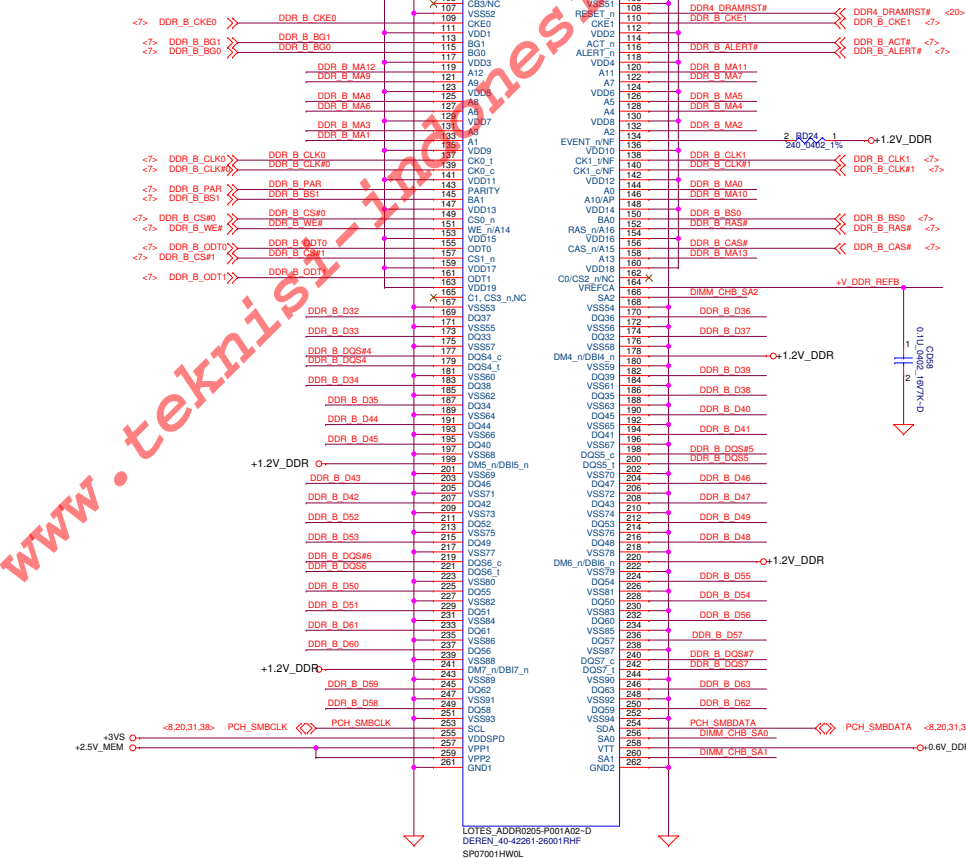
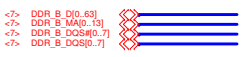
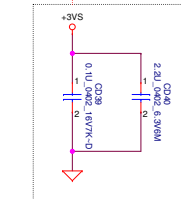
Layout Note:
Place near JDIMM2.257,259



Layout Note:
Place near JDIMM2

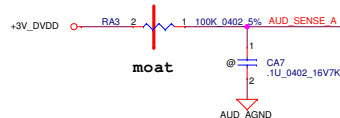
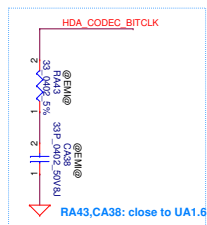
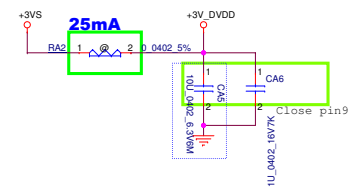
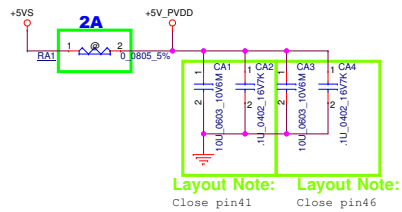


Layout Note:
Place near JDIMM2.255

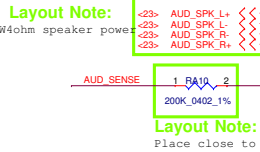
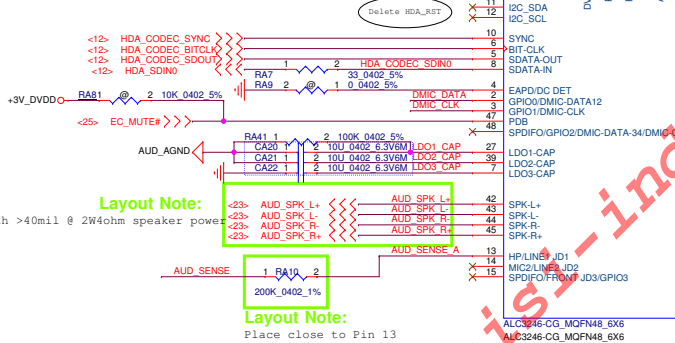
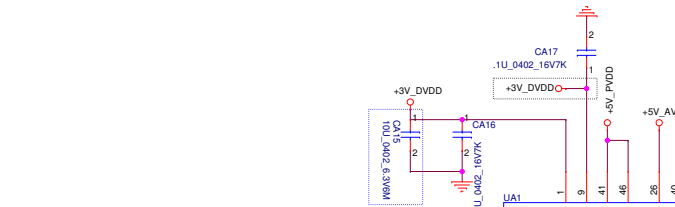
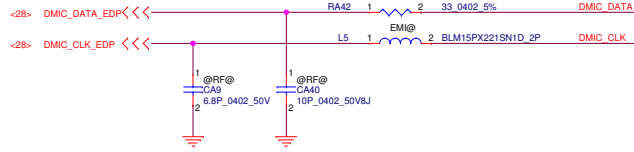
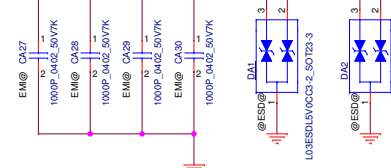
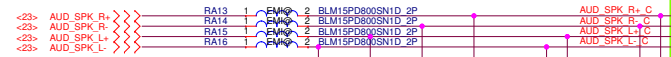


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				Date	Tuesday, November 13, 2018
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Main Func = Audio

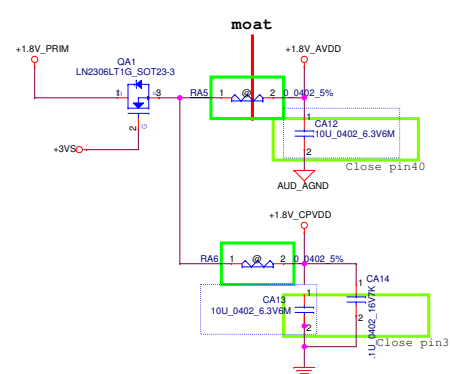
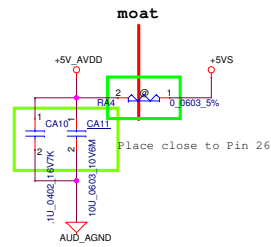
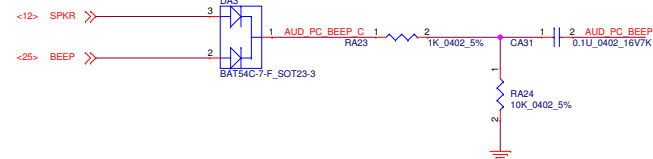


Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

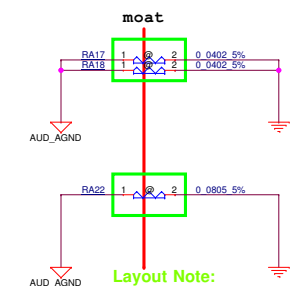


Speaker

CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



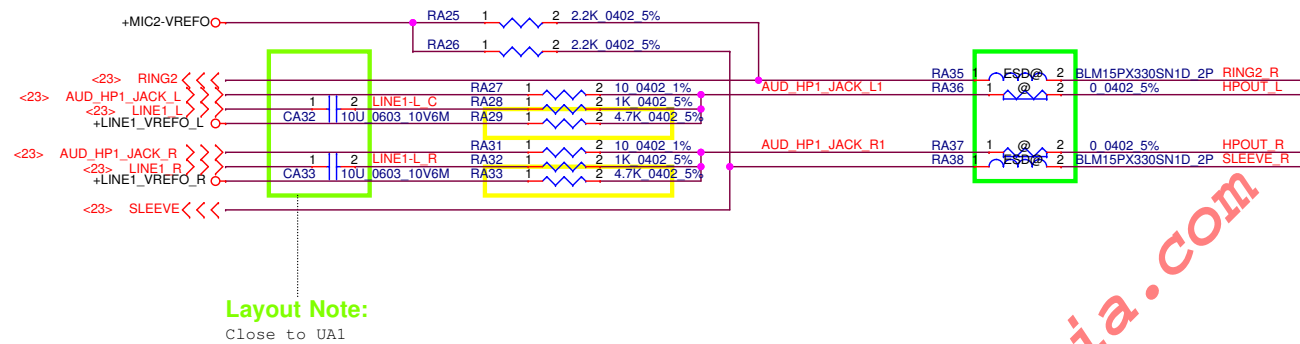
Layout Note: Width>40mil, to improve Headphone Crosstalk noise Change it to sharp will be better. Add 2 vias (>0.5A) when trace layer change.



Layout Note: Tied at point only under Codec or near the Codec.

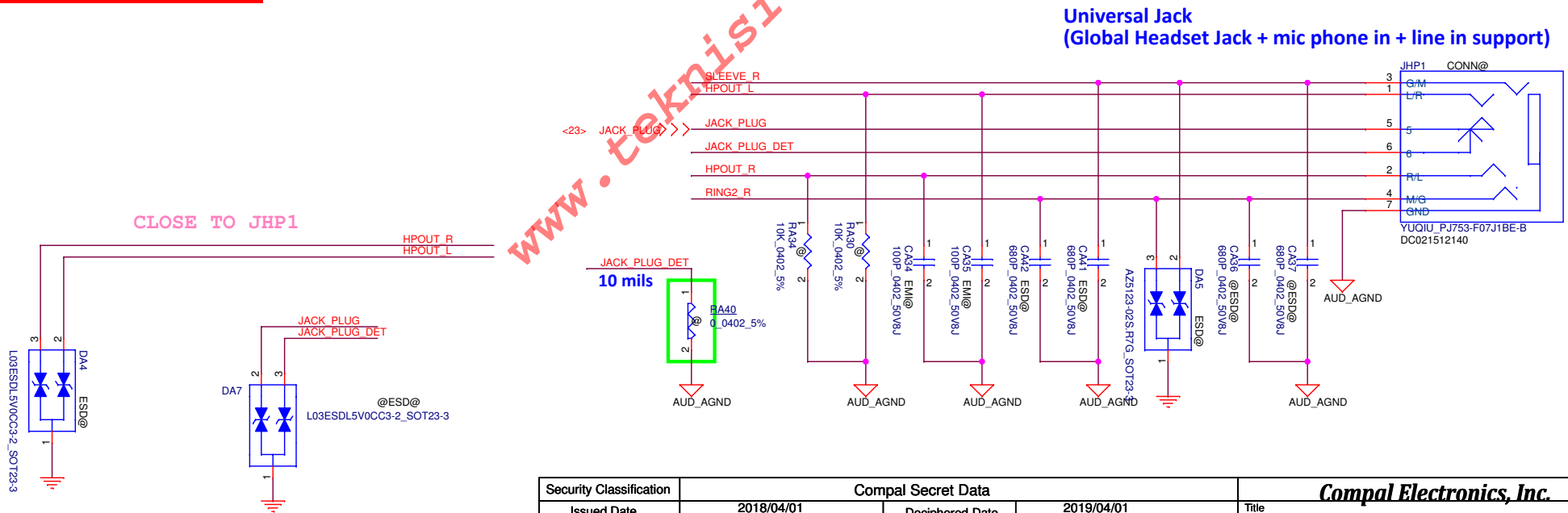
Place on the moat between GND & GNDA.

Main Func = Audio Jack



Universal Jack
(Global Headset Jack + mic phone in + line in support)

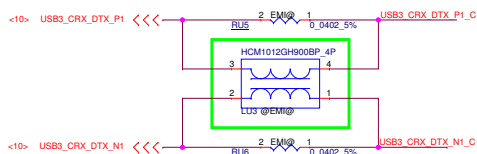
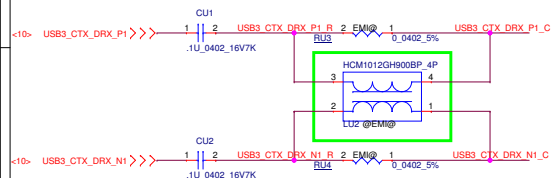
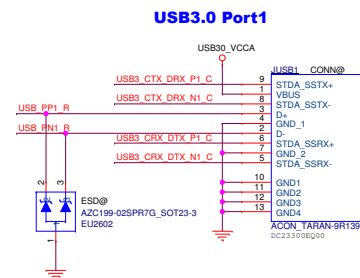
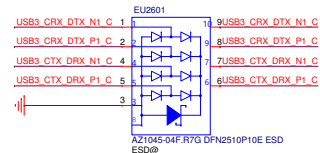
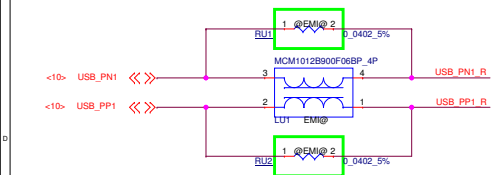
Main Func = Audio Jack



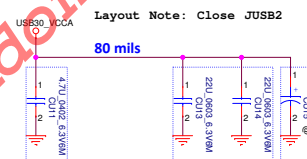
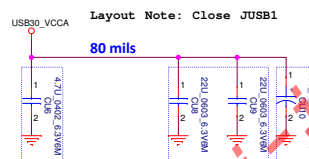
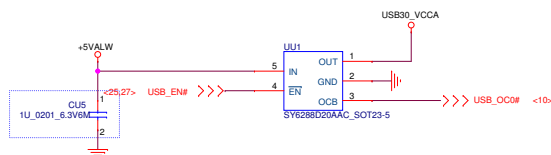
Universal Jack
(Global Headset Jack + mic phone in + line in support)

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Size		Document Number		Rev	
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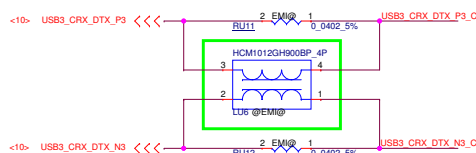
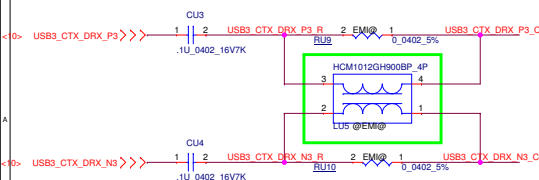
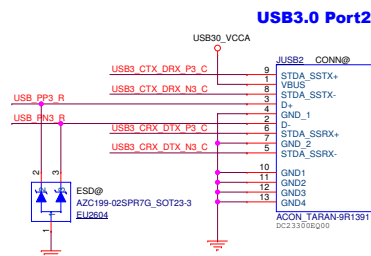
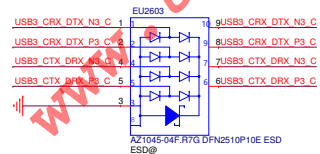
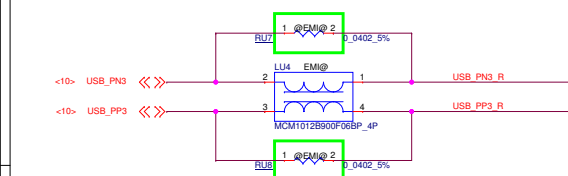
Main Func = USB3.0 Port1



Maximum Output Current 2A

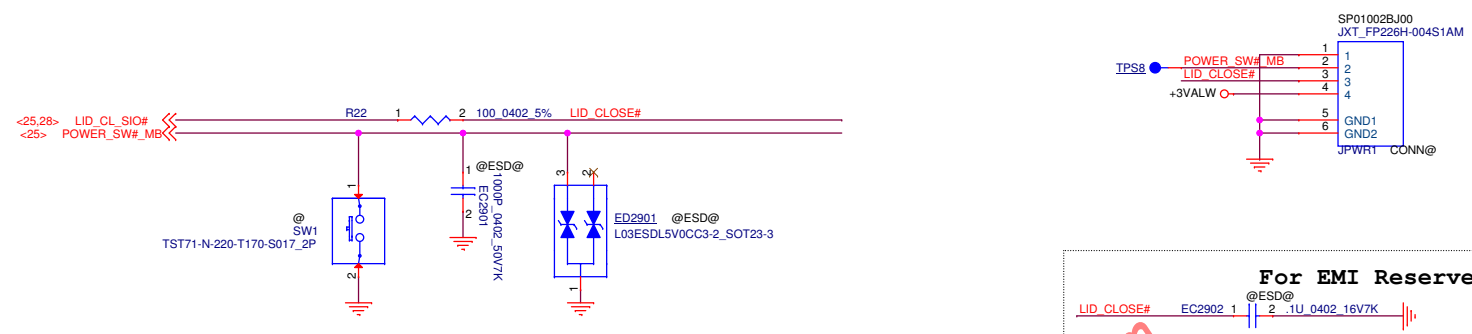


Main Func = USB3.0 Port2



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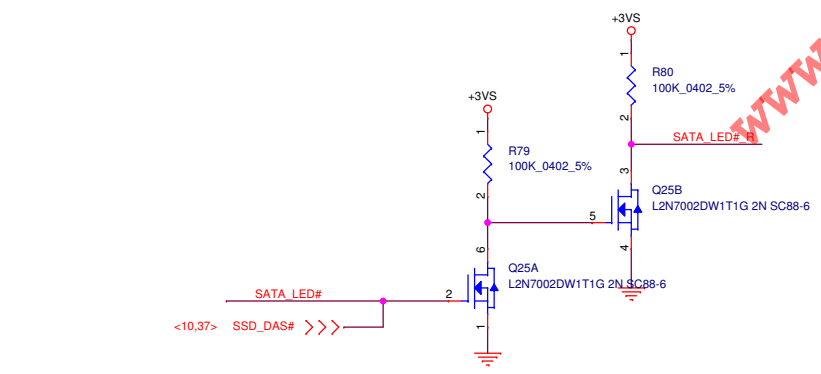
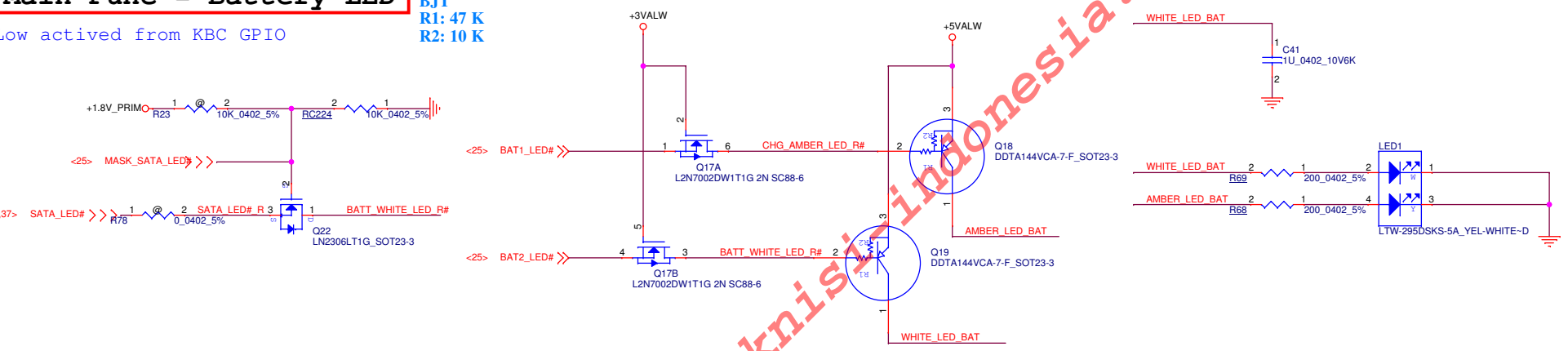
Main Func = Power BTN



Main Func = Battery LED

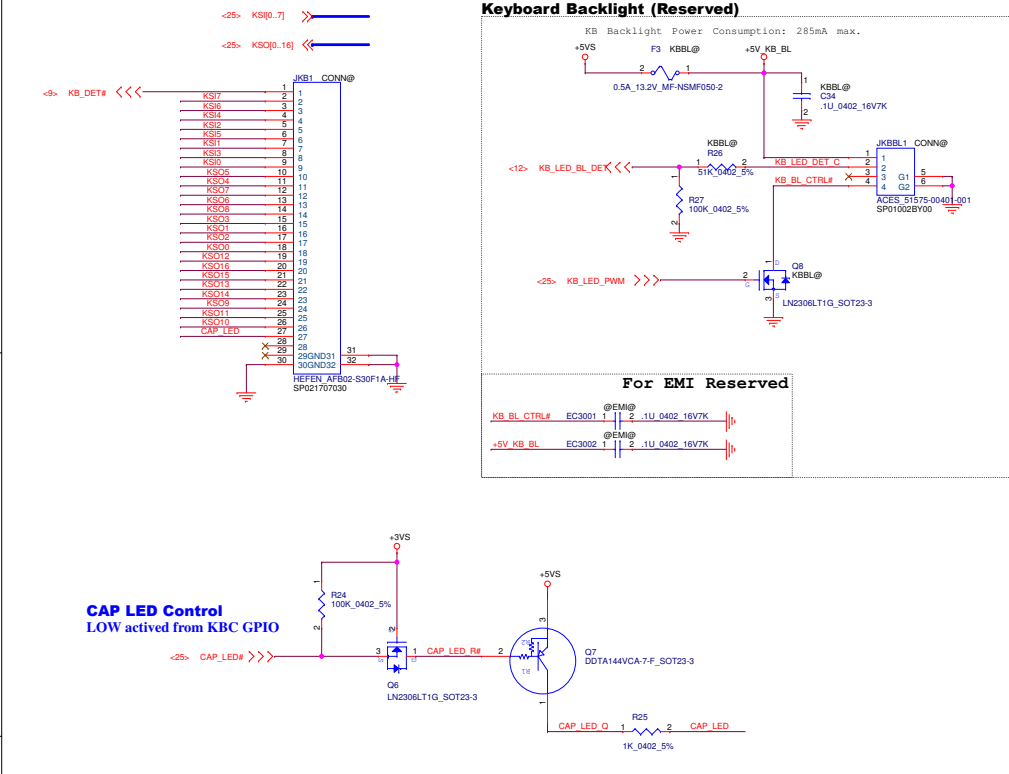
BJT
R1: 47 K
R2: 10 K

Low actived from KBC GPIO

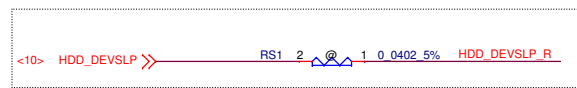
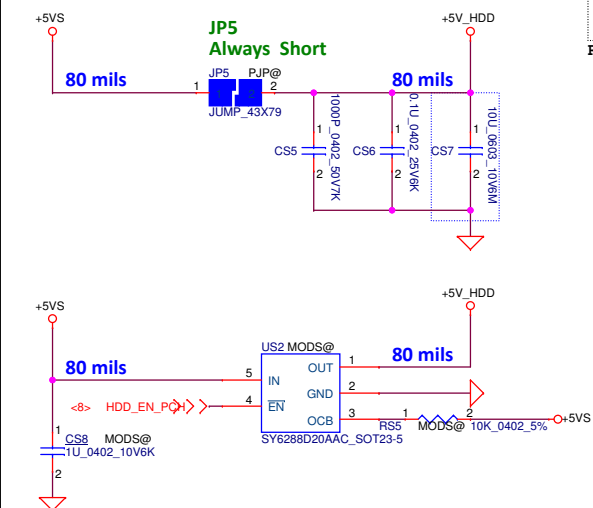


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				29	65

Main Func = K



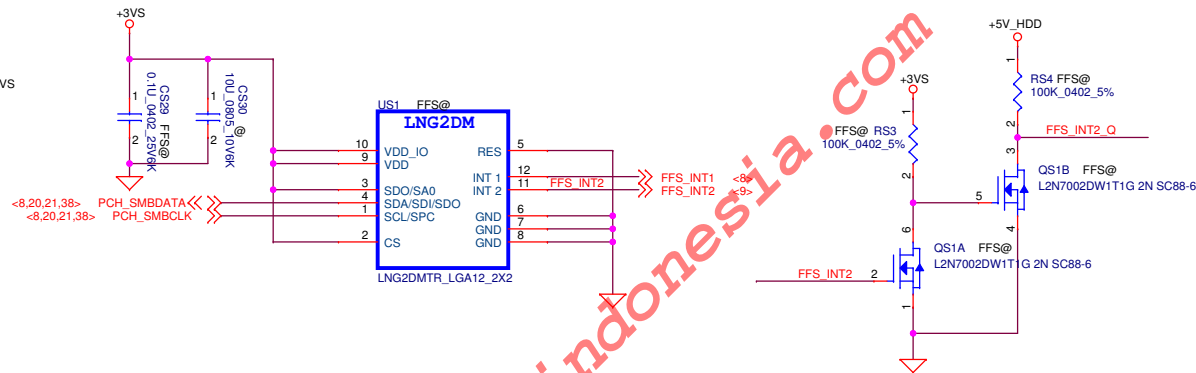
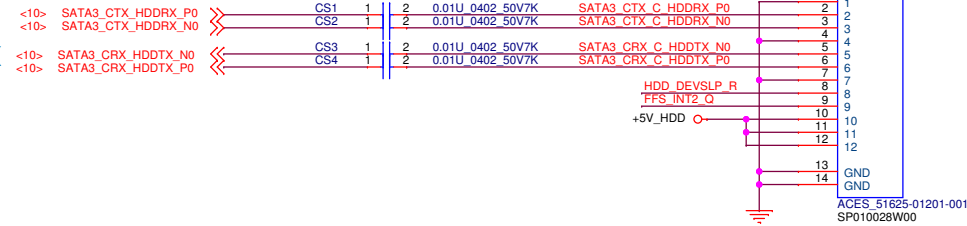
Main Func = HDD&FFS



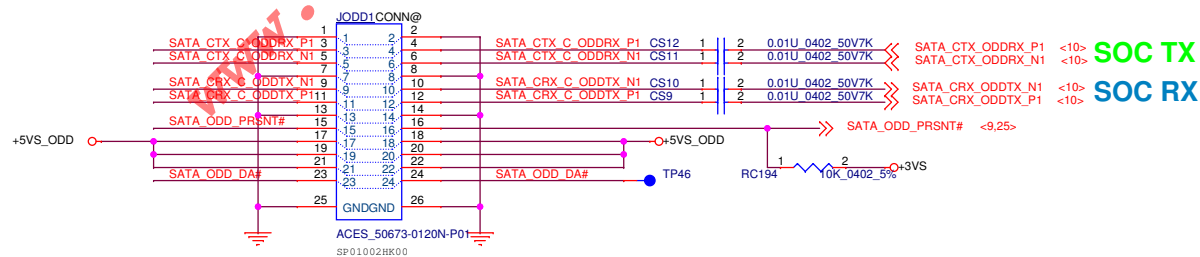
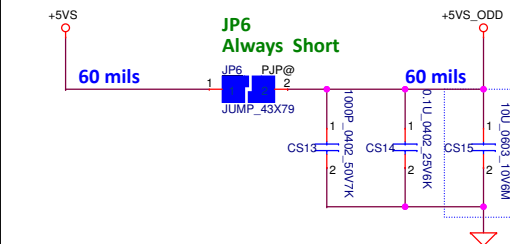
Reserve, refer to M15 EE Implementation Requirements

SOC TX

SOC RX



Main Func = ODD

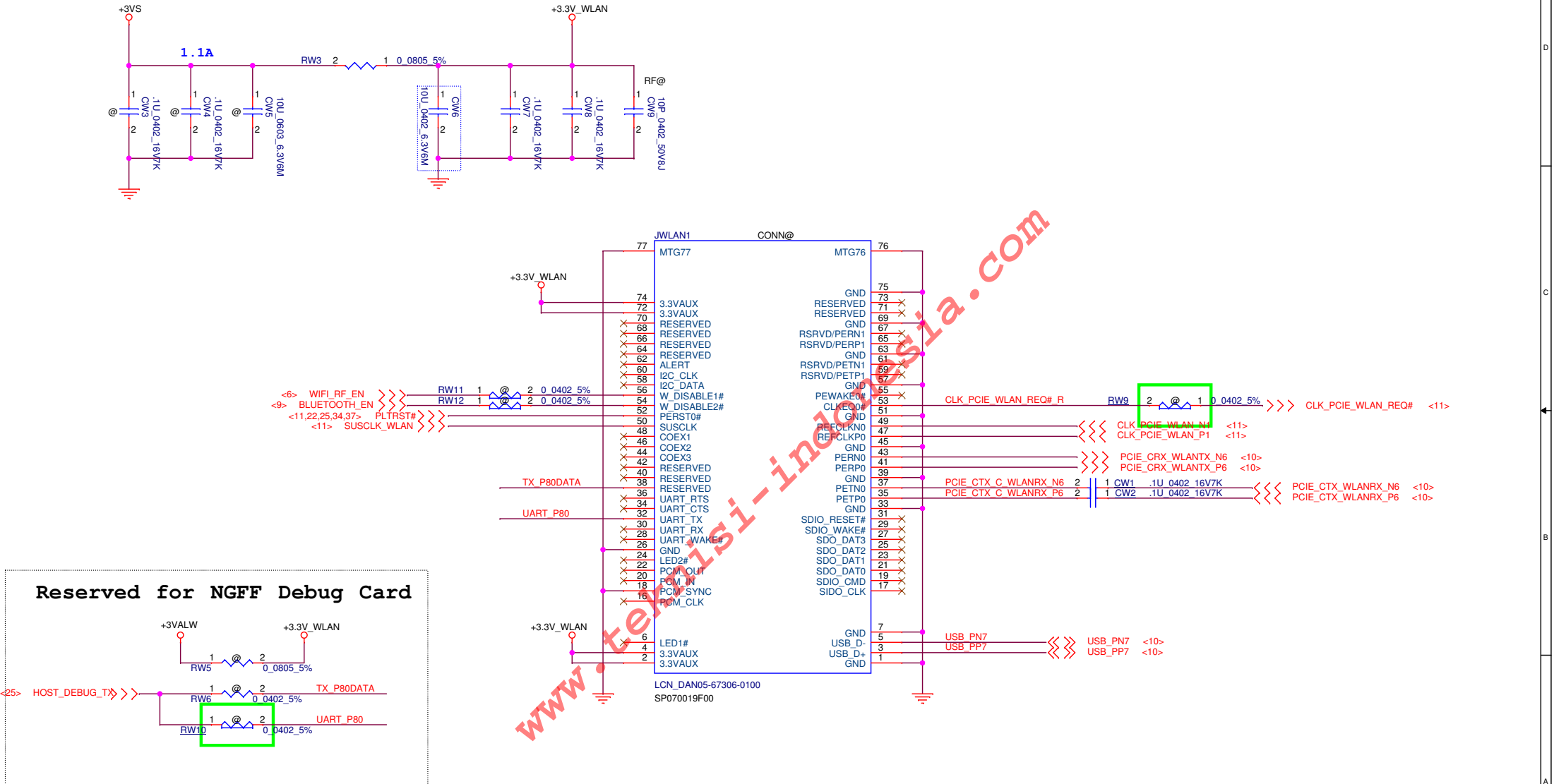


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	

CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSENT	P1	8
5V	P2	9
5V	P3	10
Attention	P4	12
GND	P5	
GND	P6	

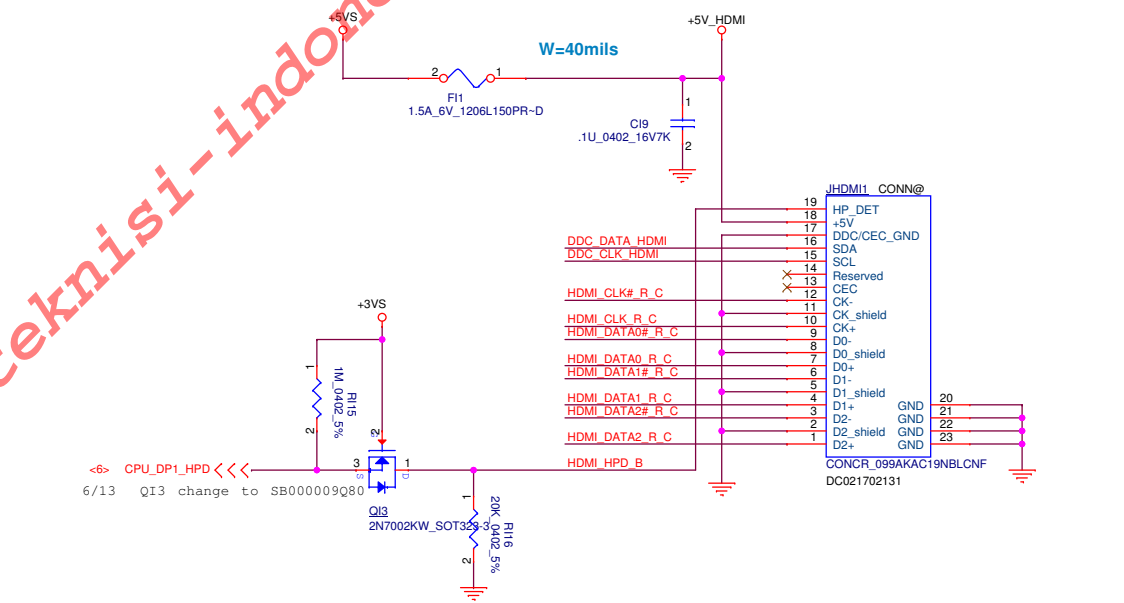
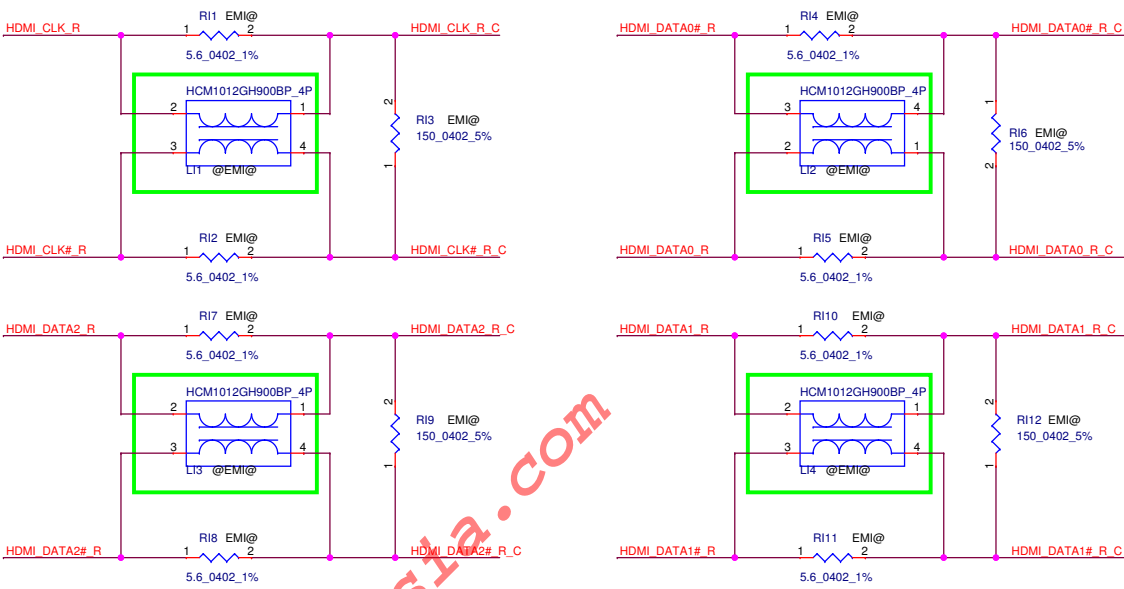
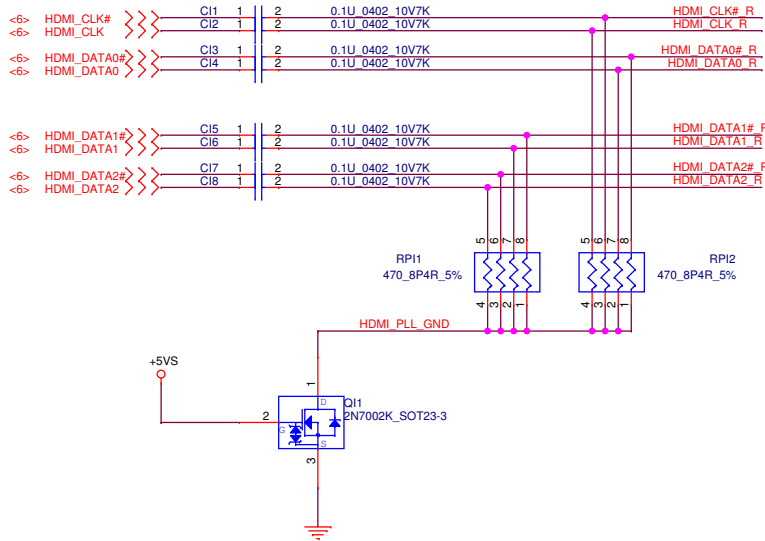
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Main Func = WLAN A Key CONN



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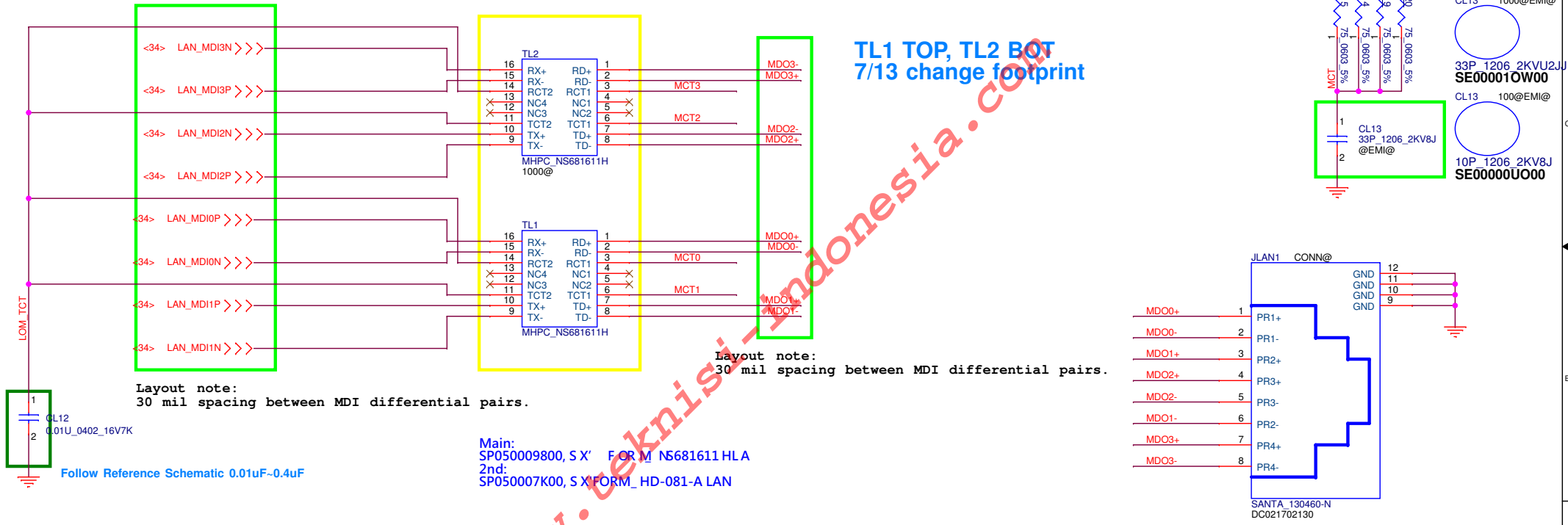
Main Func = HDMI



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						Size		Document Number		Rev	
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LAN TransFormer (Giga & 10/100 co-layout)

Dont use SP050006H00 on Giga LAN SKU due to EMI test failure.



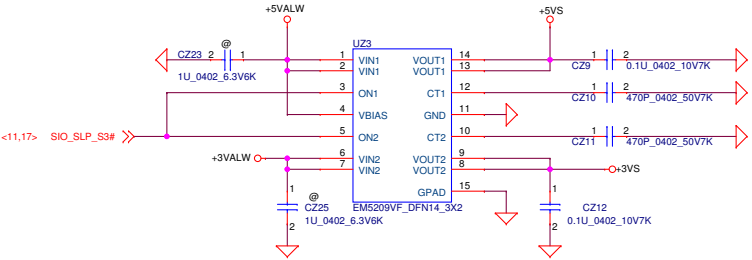
Layout note:
30 mil spacing between MDI differential pairs.

Main:
SP050009800, S X' F OR M NS681611 HLA
2nd:
SP050007K00, S X' FORM_ HD-081-A LAN

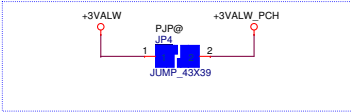
Follow Reference Schematic 0.01uF~0.4uF

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				Size	Document Number
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+5VS/+3VS for System



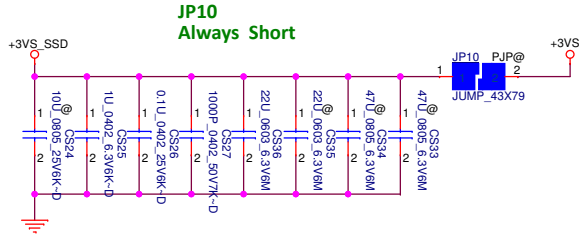
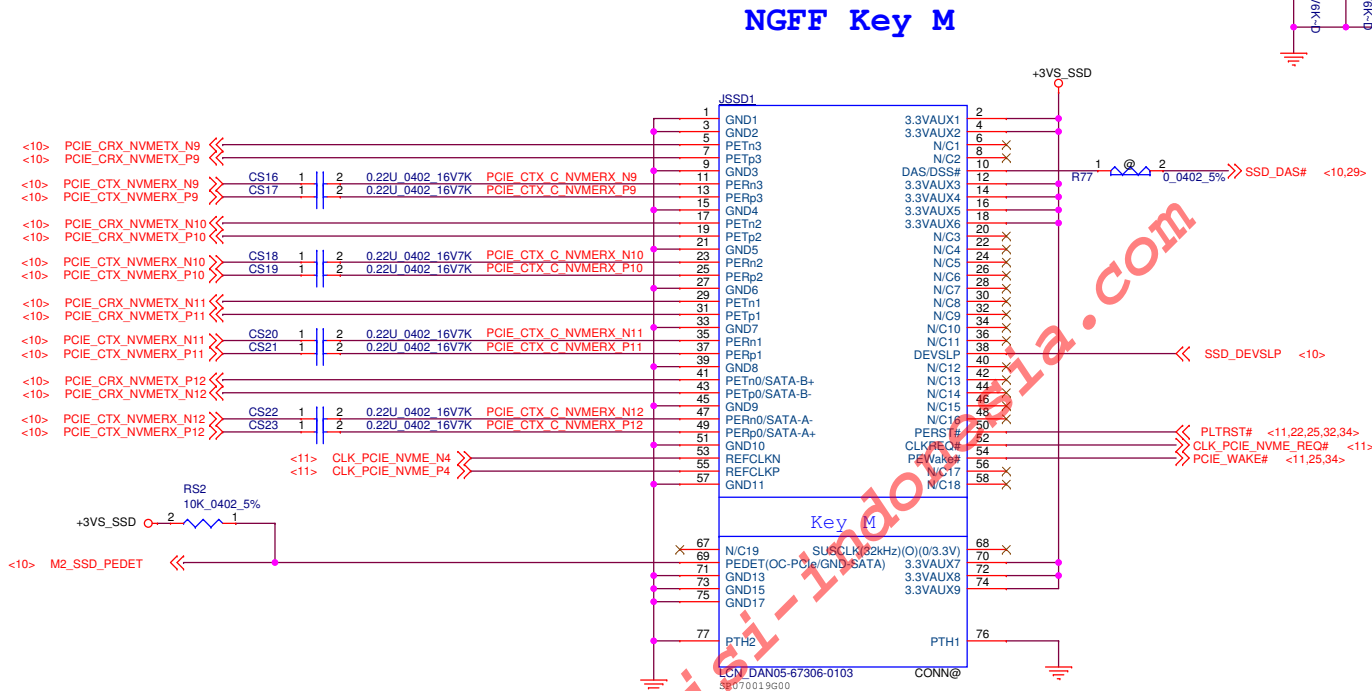
+3VALW_PCH for System



JP4 Short
for NON-DS3

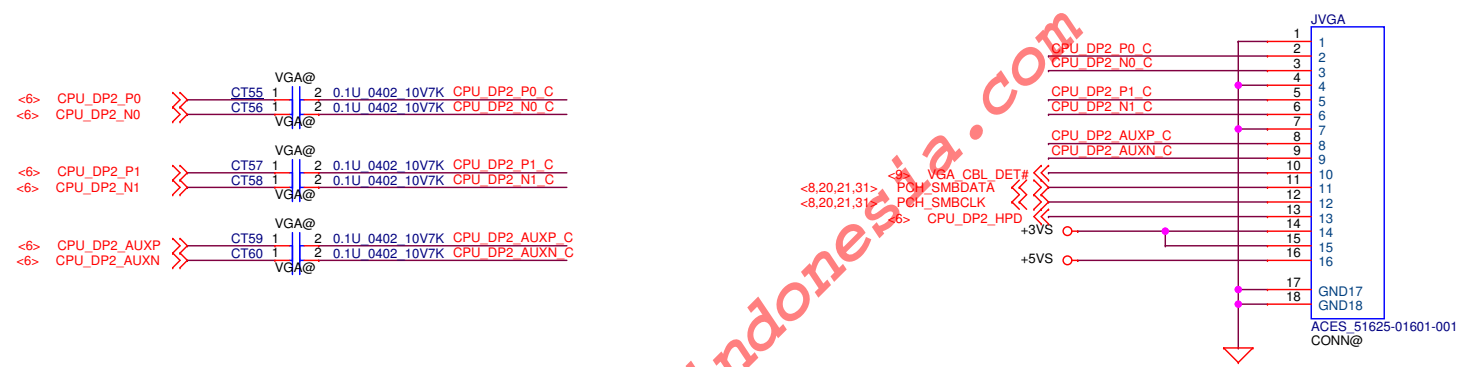
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PEDET	Module Type
0	SATA
1	PCIE

Main Func = VGA/B



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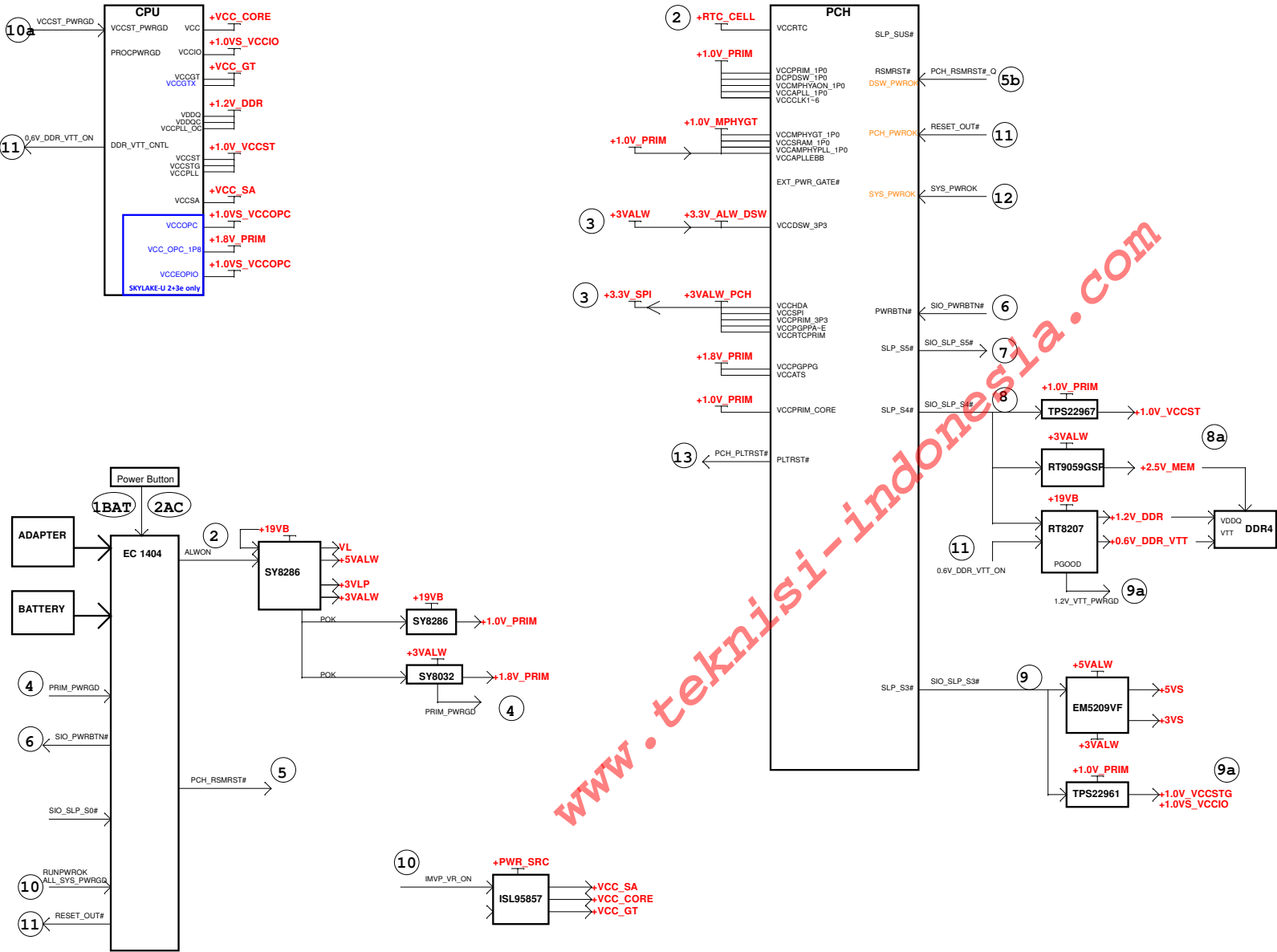
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				Size	Document Number	Rev
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				Sheet	39	of 65

5					4					3					2					1				
D																								
C																								
B																								
A																								

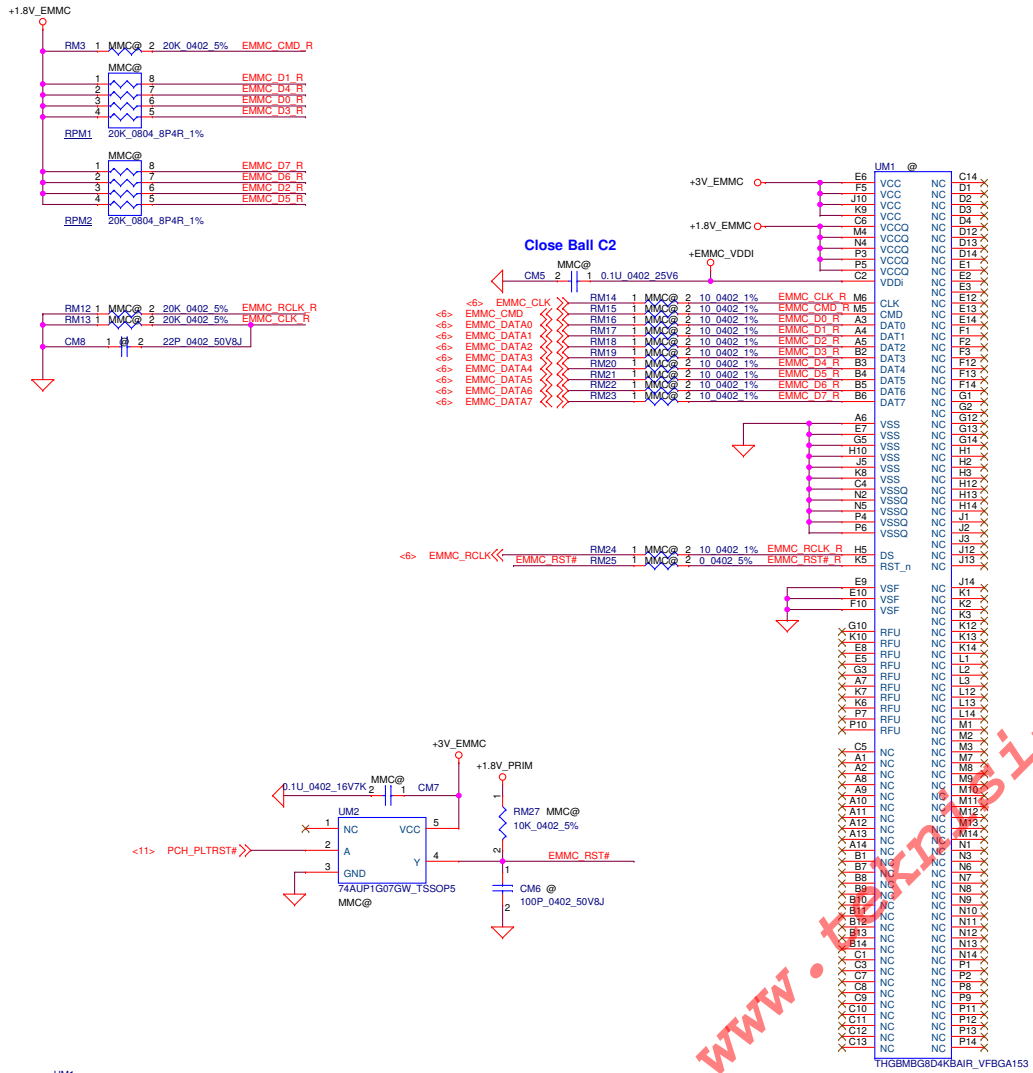
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						Size		Document Number		Rev	
						LA-G714P				1.0	
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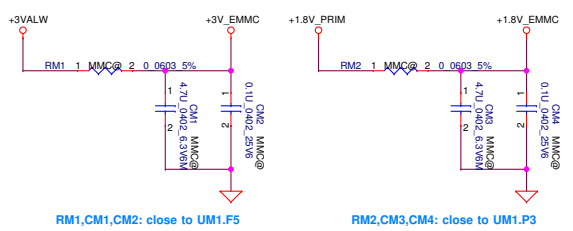
Timing Diagram for S5 to S0 mode



Main Func = eMMC



- UM1
SA00009N50L
HYNIX
HYNIX_128G@
S IC FL 128G H26M8002AMR FBGA 153P
- UM1
SA00009ML0L
SANDISK
SANDISK_128G@
S IC FL 128G SDINADF4-128G-859 TFBGA



Version Change List (P. I. R. List)

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				Document Number	
				Rev	
LA-G714P				1.0	
Date				Sheet	
Tuesday, November 13, 2018				48 01 66	

Main Func = DCIN/BATT CONN

Battery Bat 5 de

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Bat t+
PIN9 Bat t+
PIN10 Bat t+
SP021412220

ACES_50458-01001-P01_10P-T

ACES_50458-01001-P01_10P-T

ACES_50458-01001-P01_10P-T

ACES_50458-01001-P01_10P-T

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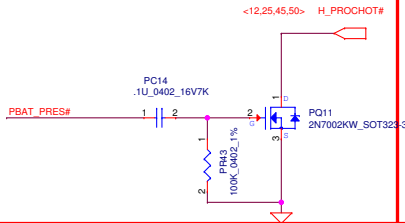
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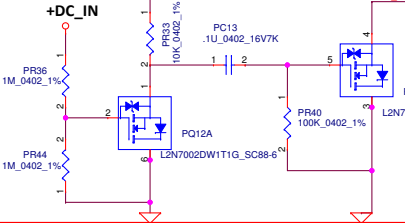
Adapter protection

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user

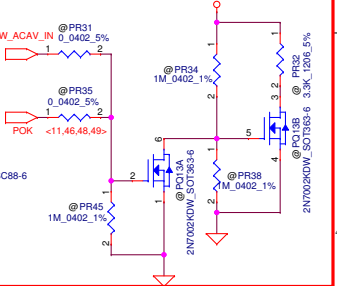


Battery protection

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC

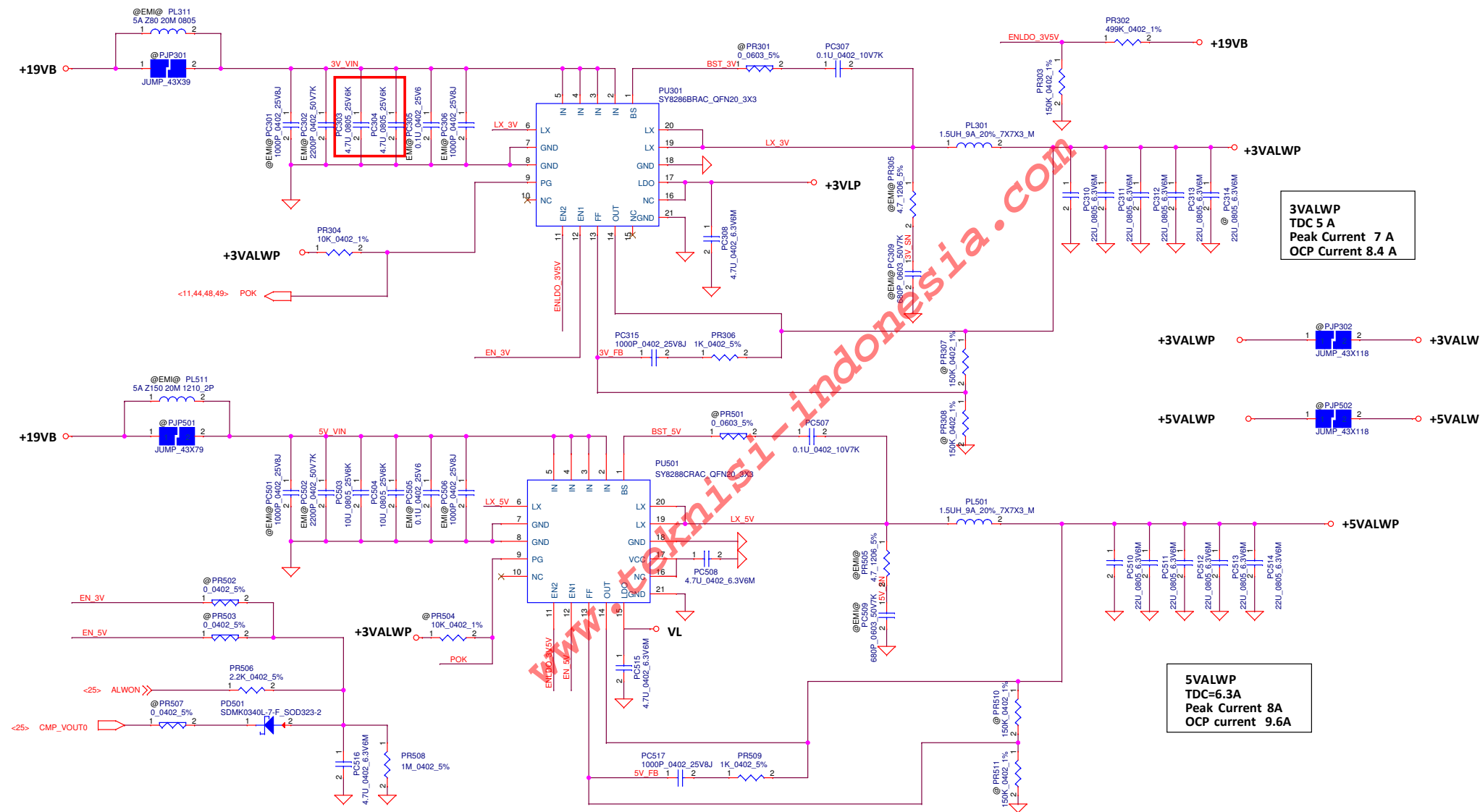


Erp lot6 Circuit



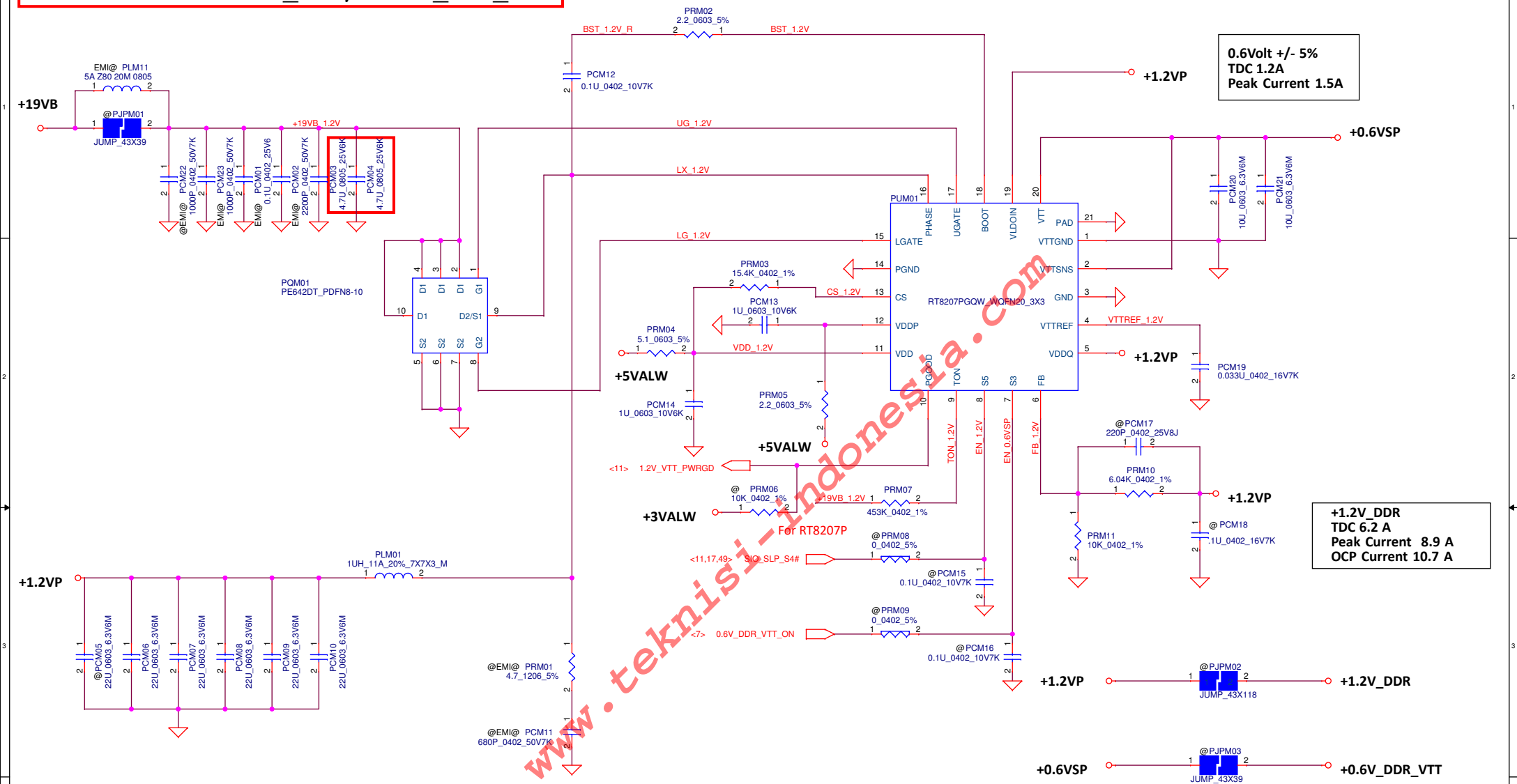
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Main Func = 3.3VALWP/5VALWP



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				Size	Document Number	Rev
					LA-G714P	0.1
Date: Tuesday, November 13, 2018				Sheet	46	of 65

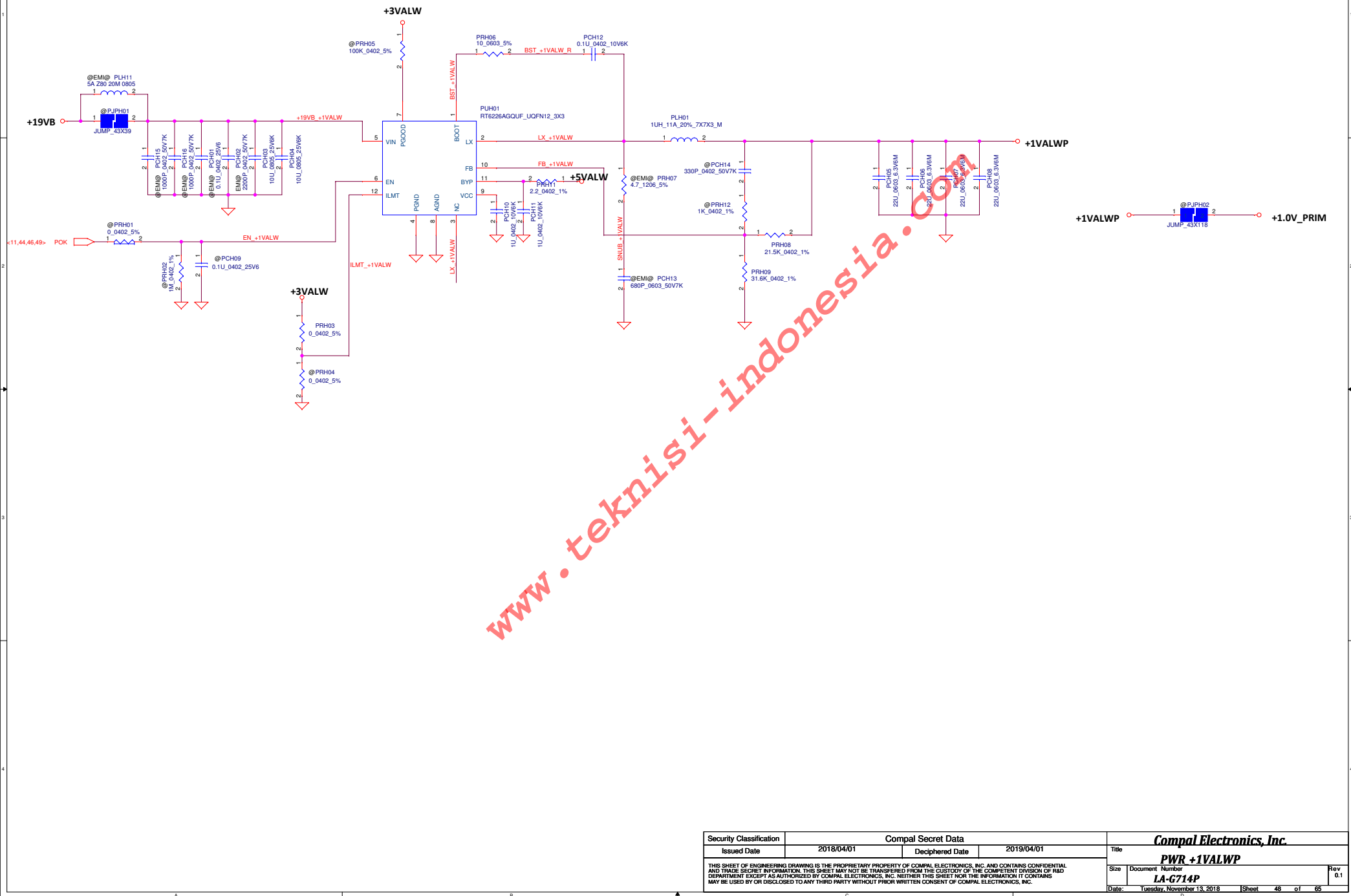
Main Func = +1.2V_DDR/+0.6V_DDR_VTT



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				Size	Document Number	Rev
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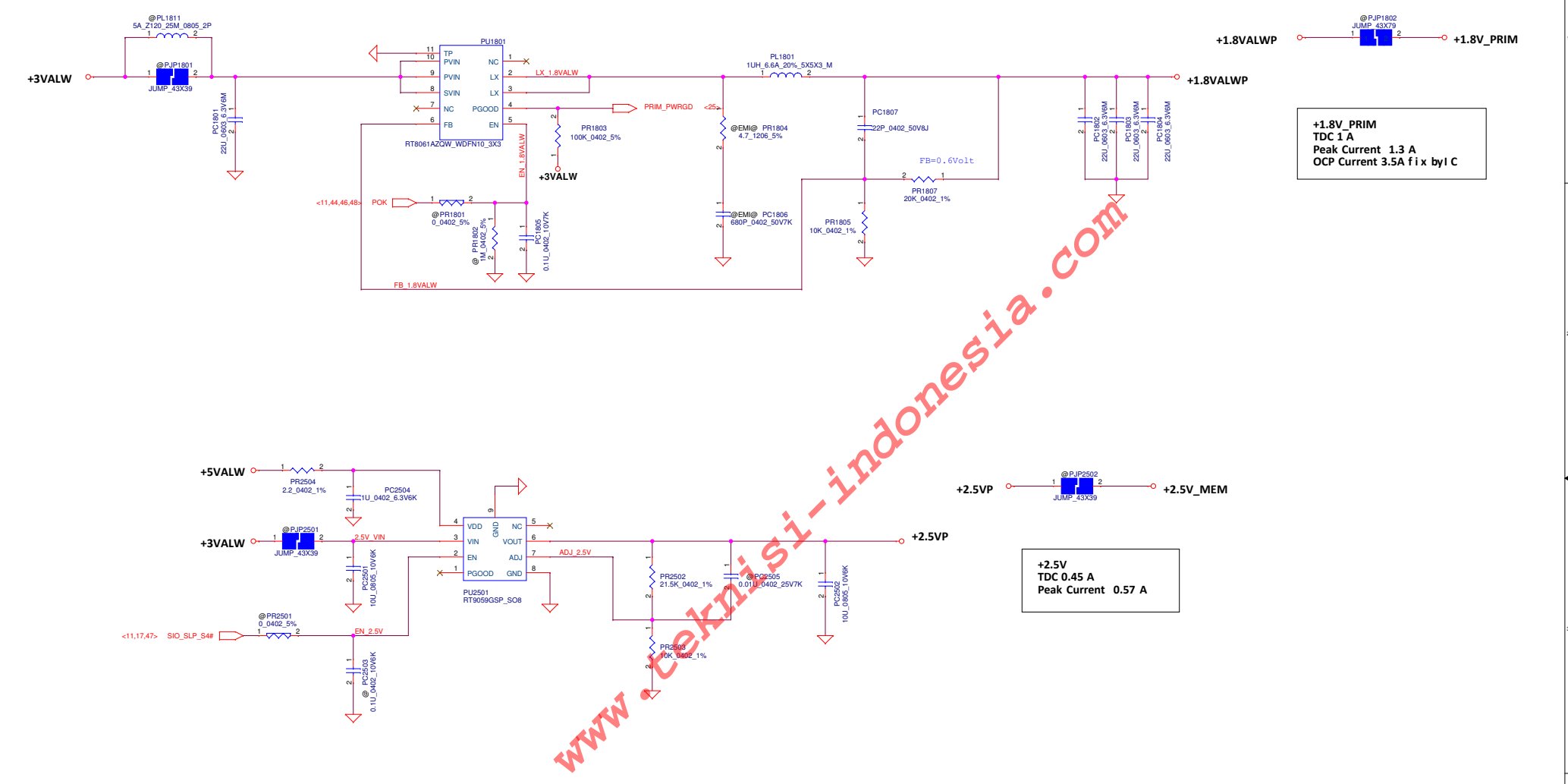
Main Func = +1VALWP

+1.0V_PRIM
TDC 5.2 A
Peak Current 6.5 A
OCP Current 9 A Fix by IC



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Main Func = +1.8VALWP / +2.5VP

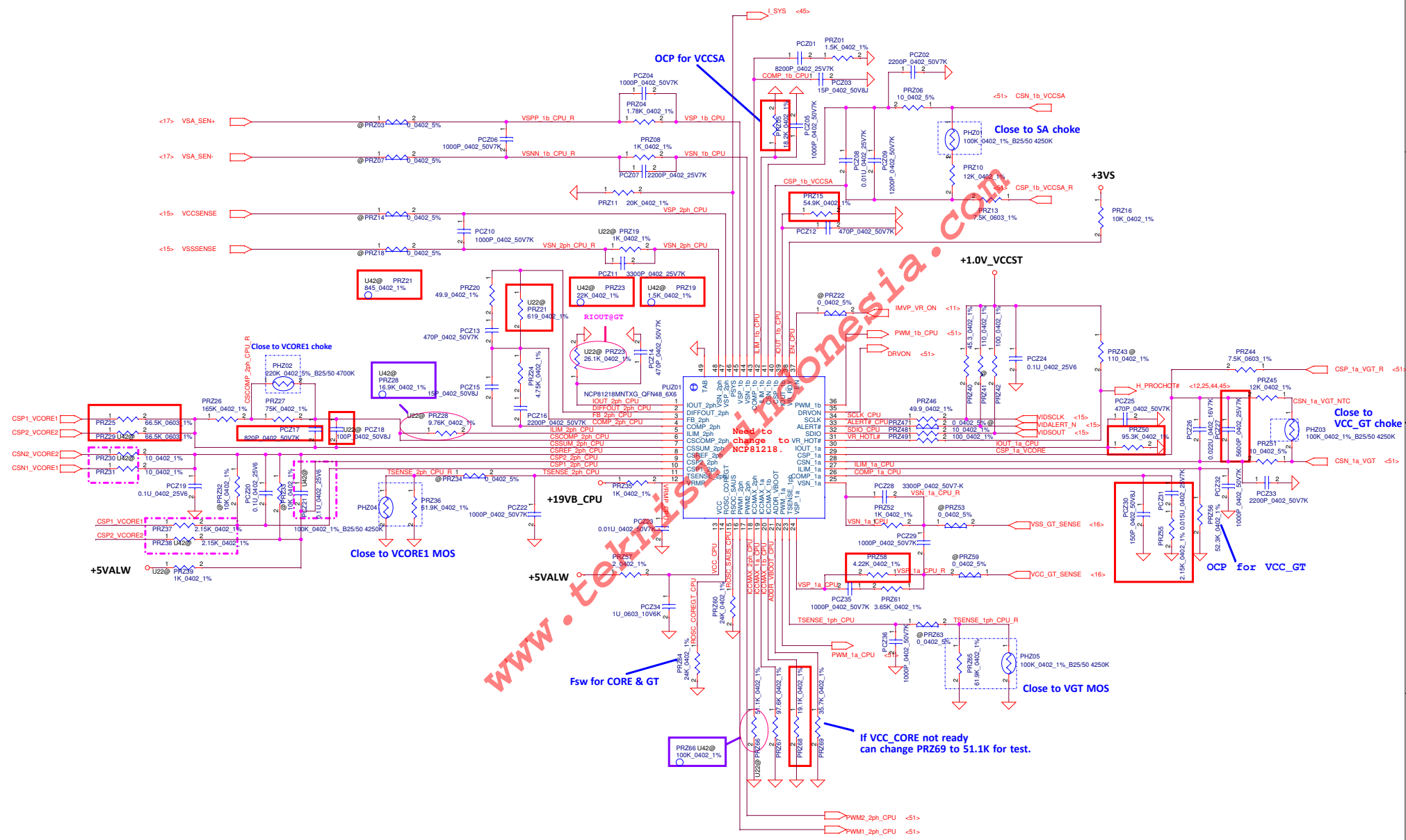


+1.8V_PRIM
TDC 1 A
Peak Current 1.3 A
OCP Current 3.5A fix by I C

+2.5V
TDC 0.45 A
Peak Current 0.57 A

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					LA-G714P	0.1
				Date:	Tuesday, November 13, 2018	Sheet 49 of 65

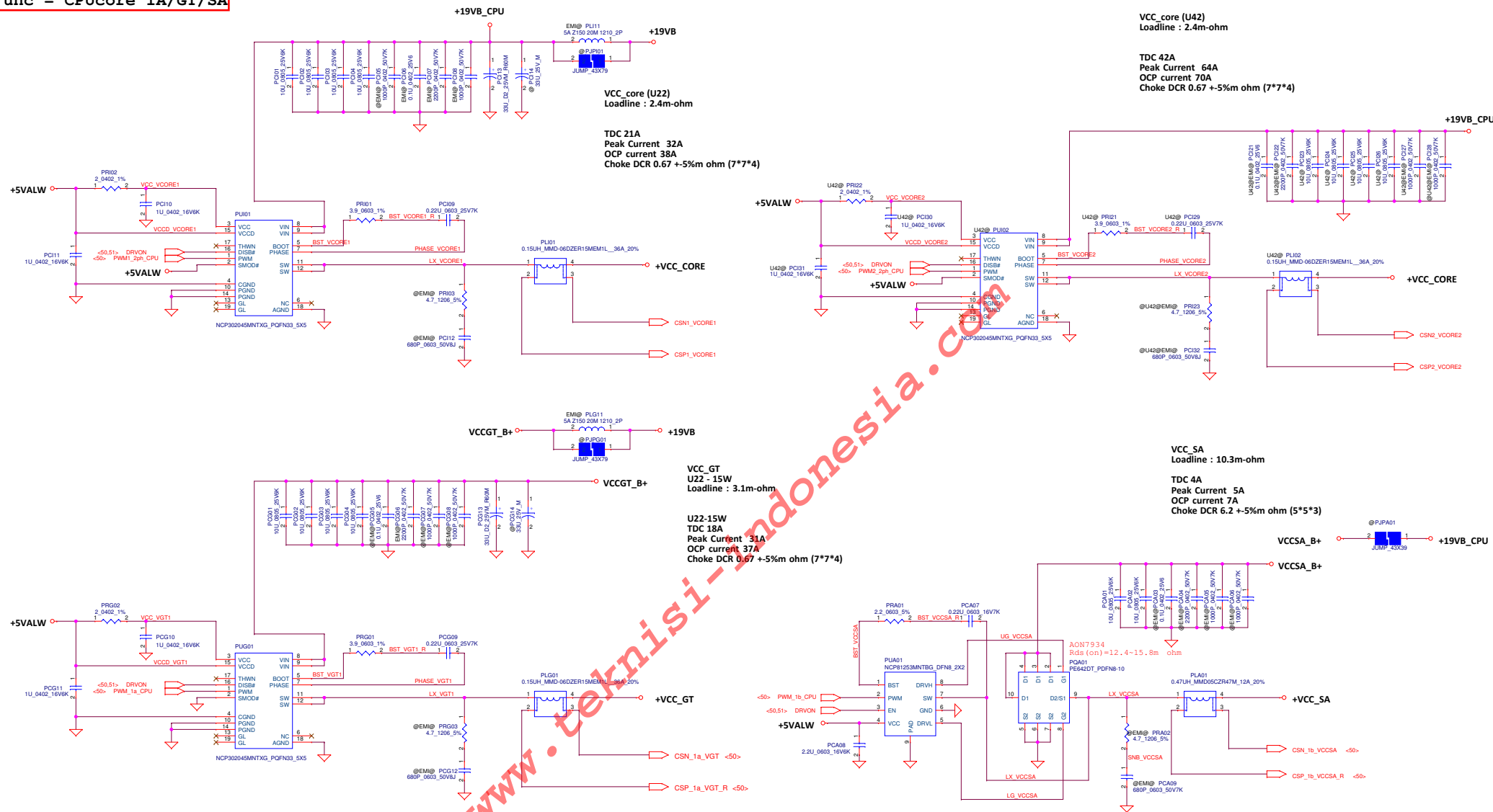
Main Func = CPU



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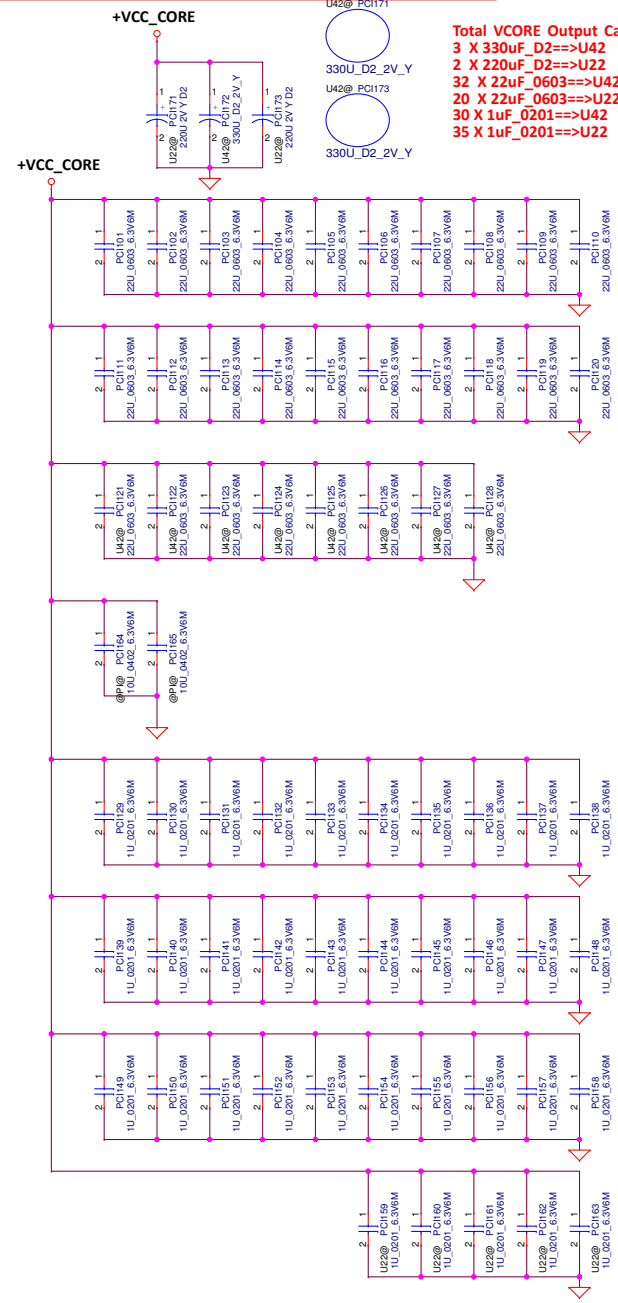
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				LA-6714P	Rev 0.1
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Main Func = CPUcore IA/GT/SA

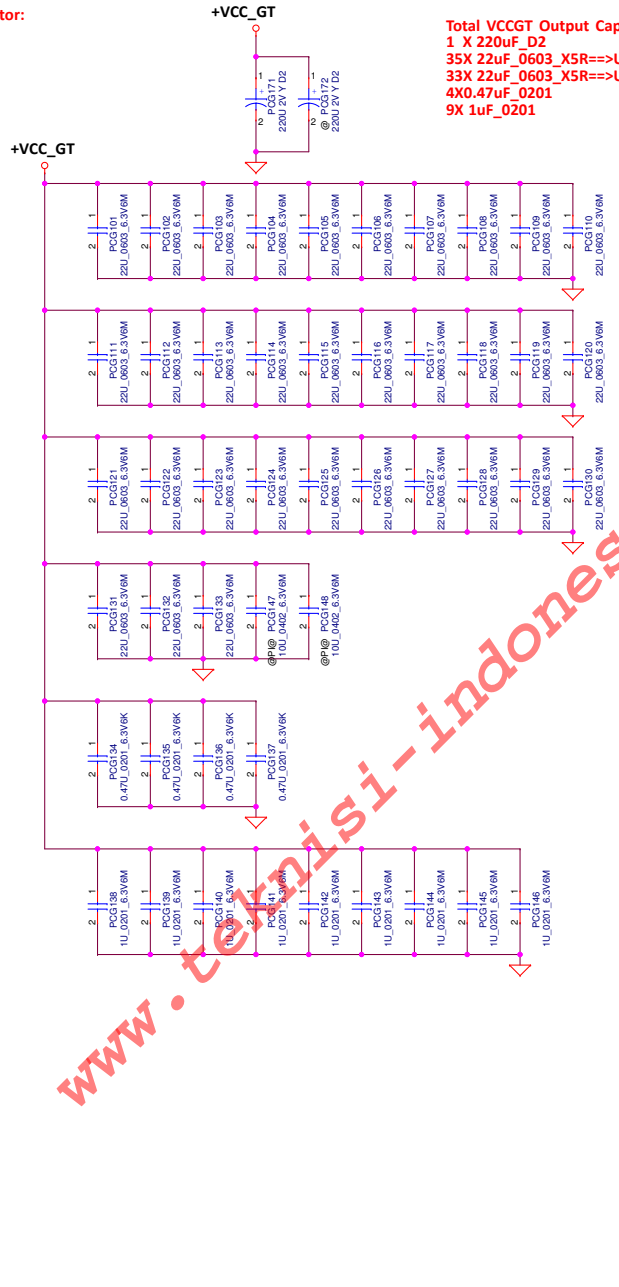


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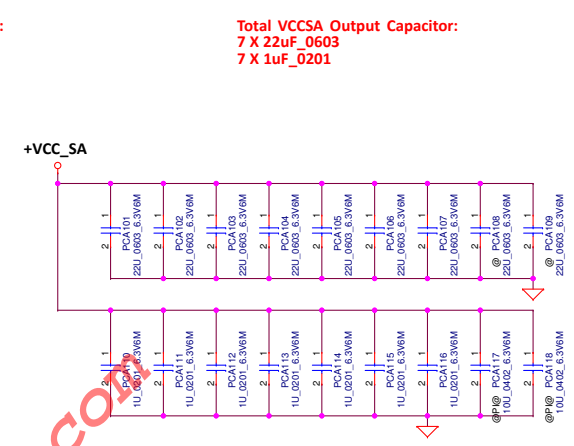
Main Func = CPU/ VGA / SA MLCC



Total VCCORE Output Capacitor:
3 X 330uF D2==>U42
2 X 220uF D2==>U22
32 X 22uF 0603==>U42
20 X 22uF 0603==>U22
30 X 1uF 0201==>U42
35 X 1uF 0201==>U22

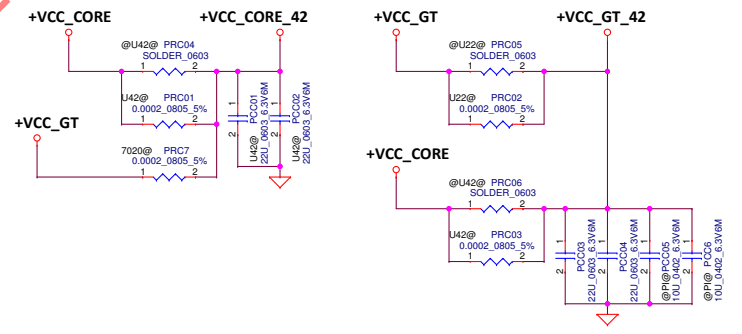


Total VCCGT Output Capacitor:
1 X 220uF D2
35X 22uF 0603_X5R==>U22
33X 22uF 0603_X5R==>U42
4X0.47uF 0201
9X 1uF 0201



Total VCCSA Output Capacitor:
7 X 22uF 0603
7 X 1uF 0201

VCC_CORE_42,VCC_GT_42 for KBL-R 4+2
VCC_GT_42 colay GT and CORE



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1	P51	PWR	20160321	COMPAL			0.1 (x00)
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3							
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6							
7							
8							

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